ML2864 Data Sheet

Version 0.0.2
Revised on Monday, April 21, 2003

CONTENTS

General Description 5
FEATURES 5
Additional Feature from ML2870 6
Block diagram 7
  Block Diagram [Logic Part] 7
  Block Diagram [Analog Part] 7
  Pin Layout55-PINS W-CSP 8
Pin Description 9
  Description of Common Mode 9
  Description of Analog Pins 11
  Parallel Access Mode 11
  Serial Access Mode 12
ABSOLUTE MAXIMUM RATINGS 13
RECOMMENDED OPERATING RANGES 13
ELECTRICAL CHARACTERISTICS 14
  DC CHARACTERISTICS 14
  AC CharacteristicsReset Timing 16
  Bus Interface at Write Cycle 17
  Bus Interface at Read Cycle 17
  Serial Interface 18
ANALOG CHARACTERISTICS 19
Timing Chart 20
  Operation of Power On 20
    Sequencer for raising VDD 20
  Bus Interface 22
    Data Read Timing 22
  Serial Interface 23
    Data Write Timing1 24
    Data Write Timing to FIFO1 25
    Data Read Timing1 26
    Data Write Timing2 27
    Data Write Timing to FIFO2 28
    Data Read Timing2 29
  Timing Chart of Functions 30
    Timing chart of PWM output 30
    Supplying clock of small amplitude 31
    Supplying Clock of digital signal 31
    Start Playback 32
    End of Playback and playback again 32
    Power down sequence during Playback 33
    Software reset timing 33
    Register Clear timing 34
    Power down sequence 35
    Power up sequence (Reset Power Down) 35
    Timing chart of analog power down 36
Power supply 37
  Timing Chart For Raising Power Supply 37

Equivalent Circuit 38
Absolute value of CLOCK PIN impedance 39
Application Circuit example (Bus Interface) 40
Application Circuit example (Serial Interface) 40
Functional Description of THE REGISTERS 42
Register Map 1 42
Register Map 2 43
Register Map 3 44
Difference Between Hardware Reset and Software Reset 45
Detailed Description of the Registers 47
ADPCM FIFO and Accompaniment Register (Read : inhibit / Write : $01h) 47
Score FIFO (Read : inhibit / Write : $03h) 48
EVENT FIFO (Read : inhibit / Write : $05h) 49
FIFO status (Read $06h : / Write : inhibit) 50
CLR Register (Read $08h : / Write : $09h) 51
CLOCK (Read $10h : / Write : $11h) 52
Pitch control (Read $12h and : / Write : $13h) 53
Tempo Control (Read $14h : / Write : $15h) 54
Power Down (Read $16h : / Write : $17h) 54
Master Clock Tuning (Read $18h : / Write : $19h) 57
MODE (Read $1Ah : / Write : $1Bh) 57
Soft Reset (Read $1Eh : / Write : $1Fh) 58
ADPCM Interrupt L (Read $20h : / Write : $21h) 59
ADPCM Interrupt H (Read $22h : / Write : $23h) 59
Score Interrupt (Read $24h : / Write : $25h) 60
Event Interrupt (Read $26h : / Write : $27h) 60
Interrupt Enable (Read $28h : / Write : $29h) 61
Request (Read $2Ah : / Write : $2Bh) 62
Status (Read $2Ch : / Write : inhibit) 63
MUSIC START (Read $30h : / Write : $31h) 64
ADPCM START (Read $32h : / Write : $33h) 65
Fsamp (Read $34h : / Write : $35h) 66
ADPCM PAN (Read $36h : / Write : $37h) 67
Volume (ADPCM) (Read $38h : / Write : $39h) 68
Port mode (Read $40h : / Write : $41h) 69
Port IO (Read $42h : / Write : $43h) 70
Port (Read $44h : / Write : $45h) 70
PWM mode (Read $46h : / Write : $47h) 71
PWMA (Read $48h : / Write : $49h) 72
PWMB (Read $4Ah : / Write : $4Bh) 72
PWMC (Read $4Ch : / Write : $4Dh) 72
PWMD (Read $4Eh : / Write : $4Fh) 72
Panel (Read $50h : / Write : $51h) 72
VIB (Read $52h : / Write : $053h) 72
Pullup (Read $54h : / Write : $55h) 72
PWM Output Select Register (Read $56h : / Write : $57h) 73
Audio Volume (Read $62h : / Write : $63h) 76
Analog Power Down (Read $66h : / Write : $67h) 77
AOUT Invert (Read $68h : / Write : $69h) 80
MIDI Implementation Chart 83
Exclusive Format 84
Transpose (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x10, 0xkk, 0xf7) 85
Main volume (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x11, 0xvv, 0xf7) 85
Touch correct (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x13, 0xtt, 0xf7) 86
Set tempo message (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x14, 0xtt1, 0xtt2, 0xf7) 86
Parameters change (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x15, 0xsw, 0xf7) 86

- Sound effects (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x18, 0xch, 0xtn, 0xf7) 87
- Relative tempo (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x19, 0xrr, 0xf7) 87
- GM System on (0xf0 0x05 0x7e 0x7f 0x09 0x01 0xf7) 87
- Master Expression (0xf0 0x06 0x5d 0x0e 0x08 0x1b ee 0xf7) 87
- Master Pan (0xf0 0x06 0x5d 0x0e 0x08 0x1c pp 0xf7) 88
- Pile Voice (0xf0 0x06 0x5d 0x0e 0x08 0x7c dco 0x00 0xf7) 88

Tone List 90

Revision History 93

ML2864 DATA SHEET

16-Tone, 64-Poly Hi-Grade PCM Sound Generator LSI

Version 0.0.2, Revised on Monday, April 21, 2003

GENERAL DESCRIPTION

ML2864 is a PCM-based hi-grade sound generator LSI, developed specifically for music ringers used in cellular/PHS phones, and plays 16 tones and 64 polyphonies simultaneously. It also has hi-grade 175 polyphonies based on General MIDI system level 1, the standard spec for PCM sound generator.

ML2864 plays standard MIDI file which is standard spec of MIDI file. It is optimum sound generator to connect to the Internet and for BGM on browser.

The on-chip FIFOs and sequencer reduce the CPU power. ML2864 is also embedded 2bit/4bit ADPCM, 8bit/16bit PCM for sound effect and LED driver with brightness-control function. It is easy to build the high quality music ringer subsystem.

FEATURES

1) On-chip high-quality GM sound set
2) 16 timbre and 64 polyphonies simultaneously
3) Ports
   Vibrator direct driver – one port
   LED direct driver with PWM – four ports
   LED direct driver for Front LCD panel – one port
   External I/O port (depending on package type)
      W-CSP: 8 ports (P7-0)
4) 3 or 4-pin serial interface or 8bit bus interface selectable
5) On-chip FIFO buffer memory
   1024bit(128Byte) FIFO for musical score data
   128bit(16Byte) FIFO for MIDI messages
   4096bit(512Byte) FIFO for ADPCM audio synthesis
6) Low power consumption at power-down: Idds = 3µA (typ.)
   Operating current: 60mA (max.)
7) Power Supply: +2.5 V ~ 3.6 V
8) Package options
   55-pin W-CSP (P-VFLGA55-5.16X4.91 –0.65-W) TBD
9) Operating Temperature: -20 ~ +85°C
10) Ordering part number :
   55-pin WCSP : ML2864HB Z060 (PbSn, Tape & Reel)
   ML2864HB Z03B (Lead Free, Tape & Reel)

ADDITIONAL FEATURE FROM ML2870

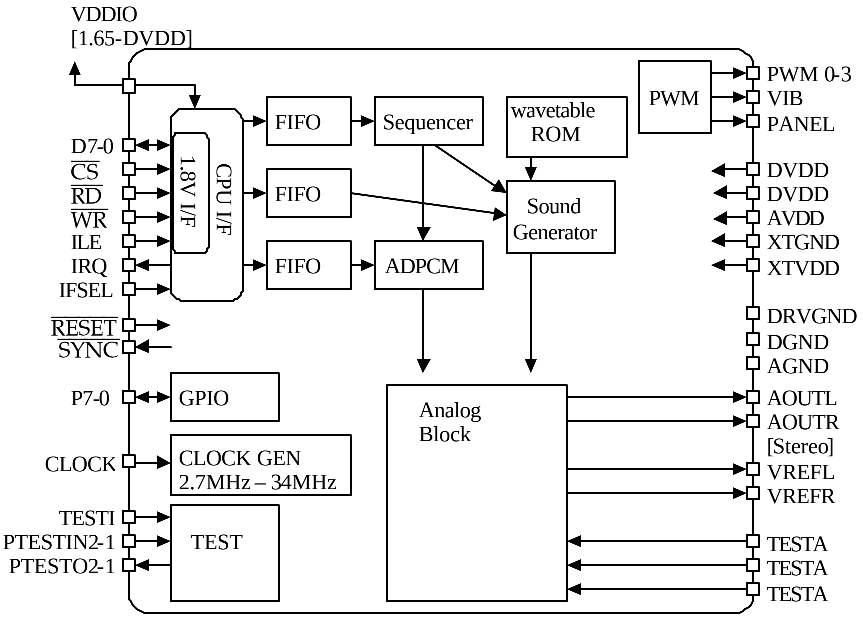
Follows are additional feature of ML2864 from ML2870.

Table 1

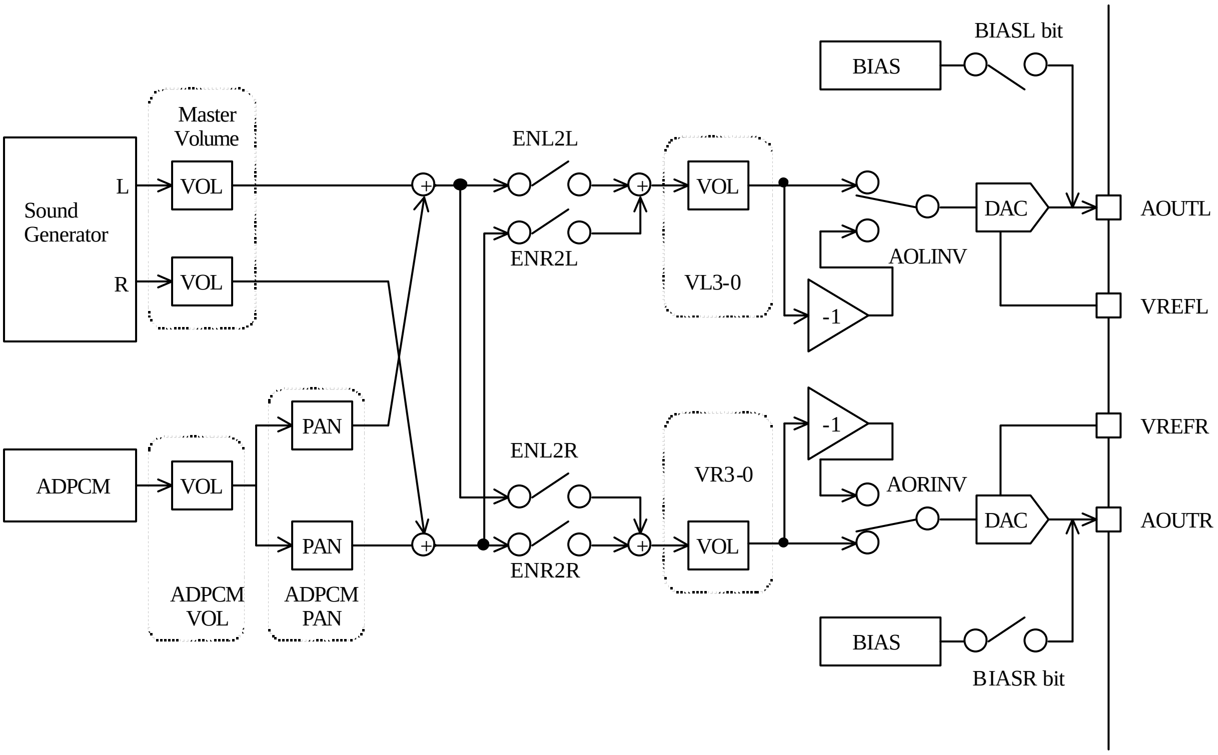
Items	ML2870	ML2864
Audio Output Voltage	Typical : 50mV – 200mV	Four times of ML2870 Typical : 200mV – 800mV
Serial Interface	2 type	Four type of serial interface embedded
DIPH/DOPH	-	Add these pin due to decision of serial I/F timing on only serial I/F pin.
Pin pitch in WCSP	0.5mm pitch	0.65mm pitch
Format of effective sound	ADPCM	ADPCM / PCM
BTL output mode	none	Embedded

BLOCK DIAGRAM

BLOCK DIAGRAM [LOGIC PART]



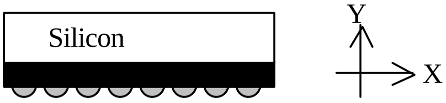
BLOCK DIAGRAM [ANALOG PART]



PIN LAYOUT55-PINS W-CSP

TBD

Bottom View



PIN DESCRIPTION

The pin description is separated into parallel, and serial interface mode and functions applying to both.

If you use the parallel interface, please refer to “Description of Common mode”, “Description of Analog Pin” and “Parallel Access Mode”.

If you use the serial interface, please refer to “Description of Common mode”, “Description of Analog Pin ”and “Serial Access Mode”.

DESCRIPTION OF COMMON MODE

Table 2: Pin description [common to parallel and serial interfaces]

WCSP	QFN	PIN NAME	VDD	I/O	Description
		$\overline{\text{RESET}}$	DVDD	I	Hardware reset signal input pin. An “L” level input to this pin initializes the LSI. After every power-on, a reset must be applied.
		IRQ	DVDD	O	Interrupt request pin. Outputs “H” level, when ADPCM FIFO or SCORE FIFO or EVENT FIFO requests next data. Threshold of request can be set for each FIFO individually. When set ISS bit of the INTERRUPT ENABLE register is set to “H”, the polarity of the interrupt is inverted.
		IFSEL	DVDD	I	IFSEL changes the CPU interface mode. CPU interface assumes bus mode, when “H”.CPU interface assumes serial mode, when “L”.
		CLOCK	DVDD	I	Master clock input. Accepts frequencies from 2.7MHz to 34MHz Refer to a detailed description in the chapter “Master Clock Frequency”.
		SYNC	DVDD	O	SYNC PIN outputs a synchronized signal controlled by Oki Original File Format called MCDF. When the SYNC pin is ”L”, CPU have to work for other function according to data in MCDF file. The function could be to send ADPCM data, display TEXT, and picture (e.g. Karaoke function). SYNC pin must be open, when MCDF format is not used. (SYNC bit in REQUEST register has similar function to SYNC pin)
		PWMA-D	Open drain	O	These are four output channels of LED with open drains. The LED brightness can be controlled by these pins with built-in PWM. Pulse width of PWM can be changed in registers. “L” level turn an LED on.
		PANEL	Open	O	Open drain output for an LCD front panel. The LED

			drain		brightness can be controlled by this pin with built-in PWM. "L" level turns front light or backlight for the LCD on.
		VIB	Open drain	O	Open drain output for a ringing vibrator. The vibration power can be controlled by this pin with built-in PWM. "L" level turns the vibrator on.
		P7-0	DVDD	I/O	Two functions are associated. One expands external ports for the CPU. Another is provision of synchronized signals from musical scores.
		TESTI	DVDD	I	TEST pin. Please connect to GND level.
		PTESTIN1 PTESTIN2	DVDD	I	For testing the WCSP and QFN assembled on print circuit. Details are described in the Application note. Make sure to connect this pin to GND ,when if is not used..
		PTESTO1 PTESTO2	DVDD	O	For testing the WCSP and QFN assembled on print circuit. Make sure to keep this pin open, when if is not used.
		AVDD	-	-	The ANALOG power supply pin. Insert a 0.1 µF or larger by-pass capacitor between the AGND and this pin.
		AGND	-	-	The ANALOG ground pin.
		DVDD	-	-	The DIGITAL power supply pin. Insert a 0.1 µF or larger by-pass capacitor between the DGND and this pin.
		DGND	-	-	The DIGITAL ground pin.
		VDDIO	-	-	The IO power supply pin. Insert a 0.1 µF or larger by-pass capacitor between the DGND and this pin.
	*	XTGND	-	-	The OSCILLATION ground pin.
	*	XTVDD	-	-	The OSCILLATION power supply pin ,as CLOCK. Insert a 0.1 µF or larger by-pass capacitor between the XTGND and this pin.
		DrvGND	-	-	Ground pin for the drivers PWM,VIB and PANEL.

DESCRIPTION OF ANALOG PINS

Table 3

WCSP	QFN	PIN NAME	VDD	I/O	Description
		AOUTL	AVDD	O	This pin is for audio output pin of left side
		AOUTR	AVDD	O	This pin is for audio output pin of right side
		VREFL	AVDD	O	This pin outputs reference voltage of AOUTL pin. It is necessary to connect 1µF of capacitor between this pin and AGND pin.
		VREFR	AVDD	O	This pin outputs reference voltage of AOUTR pin. It is necessary to connect 1µF of capacitor between this pin and AGND pin.
		TESTA	AVDD	I	For testing the LSI. Connect this pins to AGND.

PARALLEL ACCESS MODE

Table 4: Description of [parallel] interface related pins

WCSP	QFN	PIN NAME	VDD	I/O	Description
		D7-D0	VDDIO	I/O	Bi-directional data bus. When ILE pin is "H", D7-0 allow input to INDEX for register addresses. When ILE pin is "L", D7-0 allow input and output of register values of internally set indexes.
		ILE	VDDIO	I	Sets the mode of D7-0 pins to index data when ILE is "H". Data input/output from D7-0 is enabled, when ILE is "L".
		$\overline{WR}$	VDDIO	I	Write pulse input pin. This pin must be set to "L", when index and data is input to D7-0.
		$\overline{RD}$	VDDIO	I	Read pulse input pin. This pin must be set to "L", when data is output from D7-0.
		$\overline{CS}$	VDDIO	I	Write and read pulses are accepted when this pin is "L". "H" prohibits the inputs.

SERIAL ACCESS MODE

Table 5: Description of [serial] interface related pins

WCSP	QFN	PIN NAME	VDD	I/O	Description
		SDIN	VDDIO	I	Serial input for index and data
		SDOUT	VDDIO	O	8-bit serial data output.
		SCLK	VDDIO	I	Input of the data transfer clock for the SDIN and SDOUT pins.
		$\overline{CS}$	VDDIO	I	Chip select input. When “L” the SCLK data clock is accepted. The SCLK data clock is prohibited when CS=“H”.
		ARQ	VDDIO	O	Outputs “H” when ADPCM FIFO requests next data.
		SRQ	VDDIO	O	Outputs “H” when SCORE FIFO requests next data.
		ERQ	VDDIO	O	Outputs “H” when EVENT FIFO requests next data.
		DIPH	VDDIO	I	DIPH pin defines timing which the SDIN data is latched by SCLK. Input timing of serial interface depend on SCLK level when CSB pin is altered in addition with DIPH pin. Please decide the level of DIPH pin for detail seeing timing chart of serial interface.
		($\overline{RD}$),($\overline{WR}$), (ILE)	VDDIO	I	Unused pins . Please connect to GND level

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	VDD	Ta=25°C	-0.3 - +5.0	V
Input Voltage 1	VIN		-0.3 – VDD+0.3	V
Power Dissipation	Pd	-	140(TBD)	°C/W
Storage Temperature	TSTG	-	-55 - +125	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	DVDD	DGND=AGND=0V	2.5 – 3.6	V
Supply Voltage	AVDD	DGND=AGND=0V	DVDD	V
Supply Voltage	VDDIO	DGND=AGND=0V Bus Interface	1.65-DVDD	V
Supply Voltage	VDDIO	DGND=AGND=0V Serial Interface	DVDD	V
Supply Voltage	XTVDD	DGND=XTGND=0V	DVDD	V
Operating Temperature	TOP	-	-20 -+85	°C
Master clock frequency	fCLK	-	2.7- 34	MHz

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

VDDIO=1.65-DVDD, DVDD=AVDD=XTVDD=+2.5V-3.6V,

DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
"H" Input Voltage	VIH	DGND=AGND=0V	VDD x 0.8	-	-	V
"L" Input Voltage	VIL	-	-	-	VDD x 0.2	V
"H" Output Voltage	VOH	IOH=-135µA	VDDx0.8	-	-	V
"L" Output Voltage	VOL	IOL=135µA	-	-	VDDx0.2	V
"H" Input Current	IIH	VIH=VDD	-	-	10	µA
"L" Input Current	IIL	VIL=0V	-10	-	-	µA
"L" Output Voltage of PWMA-D	VOL2	IOL2=20mA	-	-	0.45	V
"L" Output Voltage of VIB	VOL3	IOL3=150mA	-	-	0.45	V
"L" Output Voltage of PANEL	VOL4	IOL2=100mA	-	-	0.45	V
Input Voltage Range of PWMA-D, PANEL, VIB	-	-	0	-	3.6	V
Master clock voltage in front of an AC coupling capacity to the CLOCK pin	VCLK	AC coupling capacity depends on frequency.	400	-	-	mVp-p
TEST1 pin Pull-Down resistor value	RT1	-	20	-	500	kΩ
P7-0 pin Pull-Up resistor value	RT2	-	20	100	500	kΩ

Parameter	Symbol	Condition		Min.	Typ	Max.	Unit
Operating Current	IDDD	Sound generator (Ports no load) AOUTL/R pins : enable AOUTL/R pins : no load		-	TBD	60	mA
Standby Current	IDDS	DVDD=AVDD 3.3V	Ta=-20-+40°C	-	3	20	µA
			Ta=+40-+50°C	-	-	TBD	µA
			Ta=+50-+75°C	-	-	TBD	µA
			Ta=+75-+85°C	-	-	TBD	µA
		DVDD=AVDD 3.6V	Ta=-20-+40°C			TBD	µA
			Ta=+40-+50°C			TBD	µA
			Ta=+50-+75°C			TBD	µA
			Ta=+75-+85°C			TBD	µA
Bias Current	IBIAS	-		-	2.5	-	µA

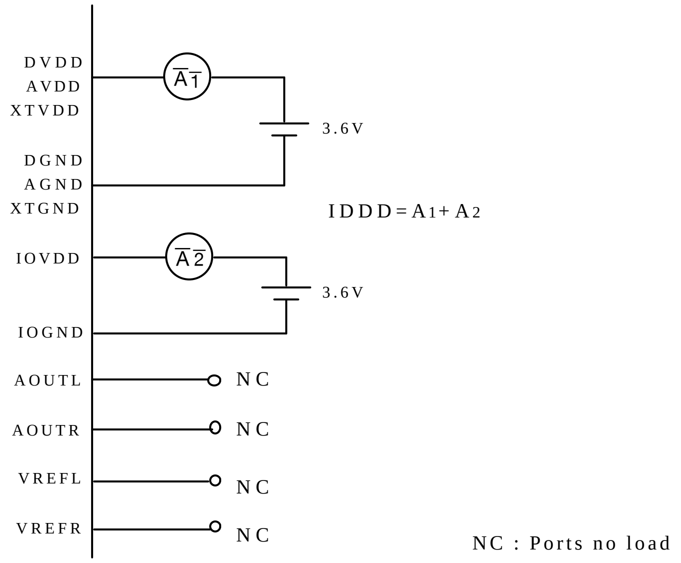
NOTE

*1 Applies to all output pins except for P7-P0 pins

*2 Applies to P7-P0 pins

*3 The following figure shows the measurement circuit.

The measurement circuit of maximum operating current



AC CHARACTERISTICSRESET TIMING

VDDIO=1.65-DVDD, DVDD=AVDD=XTVD=+2.5V-3.6V,

DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C

Parameter	Symbol	Min	Max.	Unit
RESET pulse width	tRST	1	-	us
RESET valid to CSB High	tRSC	1	-	us
CSB valid to RESET High	tINIT	1	-	us

BUS INTERFACE AT WRITE CYCLE

VDDIO=1.65-DVDD, DVDD=AVDD=XTVD=+2.5V-3.6V,
DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C
Capacitor load=30pF

Parameter	Symbol	Min	Max.	Unit
ILE valid to Write Enable Low	tIWL	10		ns
ILE valid to Write Enable High	tIWH	10		ns
Write Enable Pulse Width	tWW	25		ns
ILE valid to Chip Select Low	tICL	5		ns
Chip Select Pulse Width	tCC	50		ns
Data Valid to Write Enable Low	tDWL	50		ns
Data Valid to Write Enable High	tDWH	0		ns
Write Enable Low to Chip Select High	tWCH	25		ns
Chip Select to End of Write	tCEW	50		ns

Note : tDWL, tDWH are defined with respect to the moment CSB or WRB become High level.

BUS INTERFACE AT READ CYCLE

VDDIO=1.65-DVDD, DVDD=AVDD=XTVD=+2.5V-3.6V,
DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C
Capacitor load=30pF

Parameter	Symbol	Min	Max.	Unit
Read Enable Low to Data Valid	tRLDV	-	85	ns
Chip Enable Low to Data Valid	tCLDV	-	85	ns
Read Enable High to Data Transition	tRHDT	-	85	ns
Chip Enable High to Data Transition	tCHDT	-	85	ns

SERIAL INTERFACE

VDDIO=1.65-DVDD, DVDD=AVDD=XTVD=+2.5V-3.6V,

DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C

Parameter	Symbol	Min	Max.	Unit
Chip Select Low to SCLK Low 1	tCLSL1	100	-	ns
Chip Select Low to SCLK Low 2	tCLSL2	50	-	ns
Chip Select Low to SCLK High 1	tCLSH1	100	-	ns
Chip Select Low to SCLK High 2	tCLSH2	50	-	ns
SCLK High Pulse Width	tSH	50	-	ns
SCLK Low Pulse Width	tSL	50	-	ns
SCLK Cycle Time	tSC	100	-	ns
Input Data Valid to SCLK Low1	tIDSL1	30	-	ns
Input Data Valid to SCLK Low2	tIDSL2	30	-	ns
Input Data Valid to SCLK High1	tIDSH1	30	-	nS
Input Data Valid to SCLK High2	tIDSH2	30	-	nS
Chip Select High to SCLK Low 1	tCHSL1	0	-	ns
Chip Select High to SCLK High 2	tCHSH2	0	-	ns
Chip Select High Pulse Width	tCH	50	-	ns
Output Data Valid to SCLK Low 1	tODSL1	-	40	nS
Output Data Valid to SCLK High 2	tODSH2	-	40	nS
Chip Enable High to Data Transition	tCHDT	-	40	nS
RESET High to Chip Select Low	tRSC	180	-	nS
RESET Pulse Width	tRST	1	-	µS
Initialize Time	tINIT		40	ms

ANALOG CHARACTERISTICS

VDDIO=1.65-DVDD, DVDD=AVDD=XTVD=+2.5V-3.6V,

DGND=AGND=XTGND=DrvGND=0V, Ta=-20-+85°C

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Full Scale Range of AOUT	VAOUT	VDD=2.5V	-	0.75	-	Vp-p
		VDD=3.0V	0.81	0.9	0.99	
		VDD=3.6V	-	1.08	-	
Load Impedance of AOUT	RAOUT	After AC coupling	7	-	-	kΩ
THD of Analog output buffer	THD	VDD=3.0V Freq=1kHz No Load	-	0.05	-	%
Output Voltage of VREFL and VREFR	VREFO	-	-	0.4xVDD	-	V
Potential deference between bias level and output signal of amplifier.	VDBA	VDD=3.0V Ta=+25°C	-40	-	40	mV

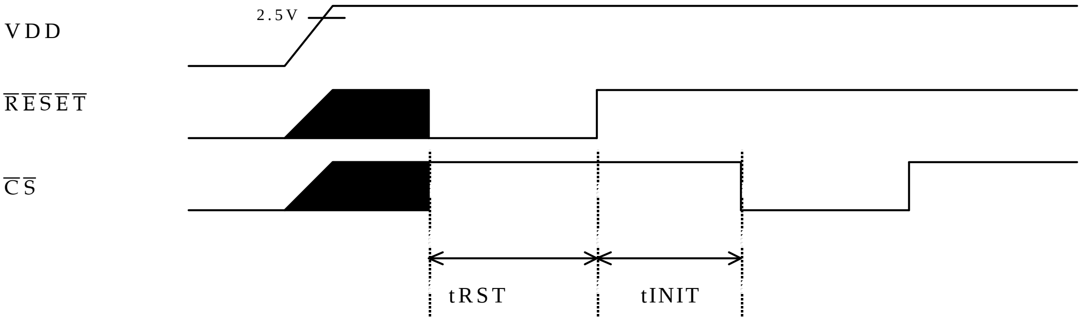
TIMING CHART

OPERATION OF POWER ON

Every time the LSI's powered on, at first input "L" level to the $\overline{\text{RESET}}$ pin to initialize the ML2870, at the timing shown below. Bringing the $\overline{\text{RESET}}$ pin to "H" level causes the LSI to initialize its internal circuit, all registers are set to their default values and the FIFO assumes EMPTY state after this initialization process.

Note that you can start accessing the serial I/F after tINIT have elapsed since bringing the $\overline{\text{RESET}}$ pin to "H" level.

Sequencer for raising VDD

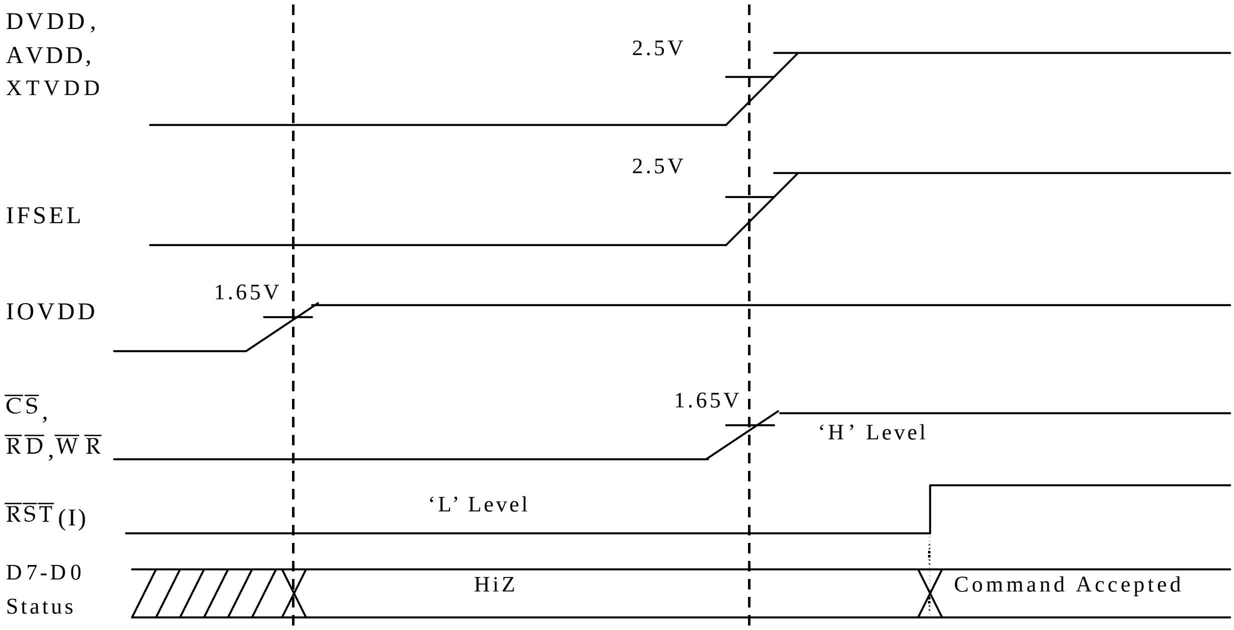


Data-Bus status at Power On

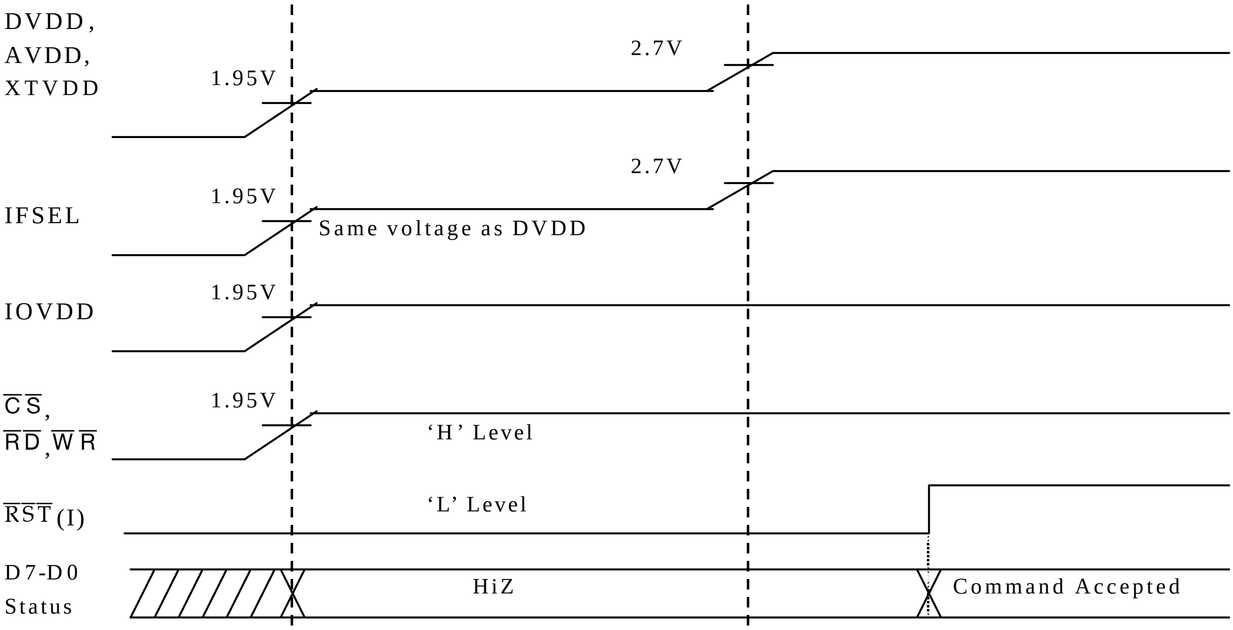
Data-Bus become high impedance under such conditions.

Condition 1 : DVDD >= IOVDD=1.65V , IFSEL = DVDD Level

This condition is applied to ML2864.

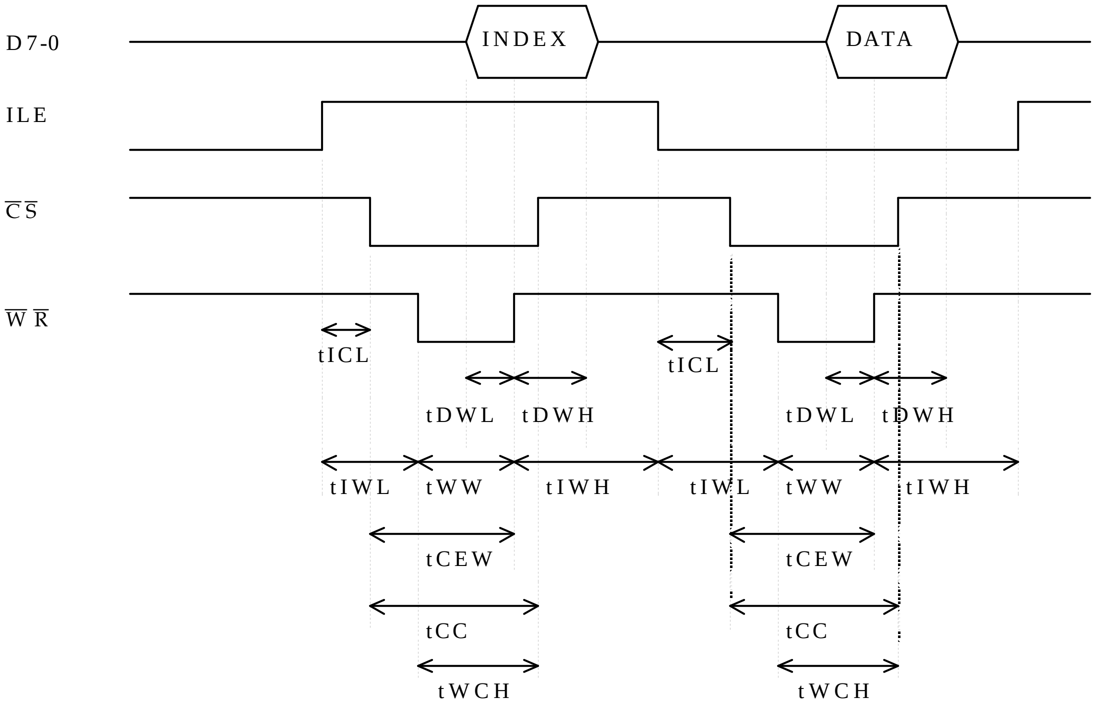


Condition 2 : DVDD >= IOVDD=1.95V , IFSEL = DVDD Level

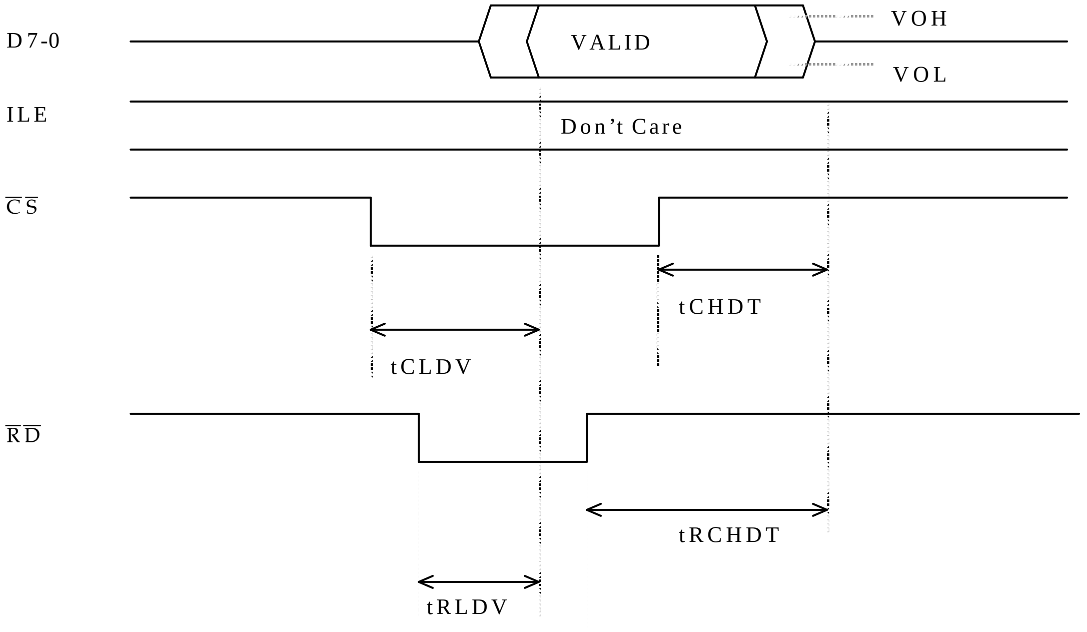


BUS INTERFACE

DATA Write TimingNote : tDWL, tDWH are defined with respect to the moment CSB or WRB become High level.



Data Read Timing



SERIAL INTERFACE

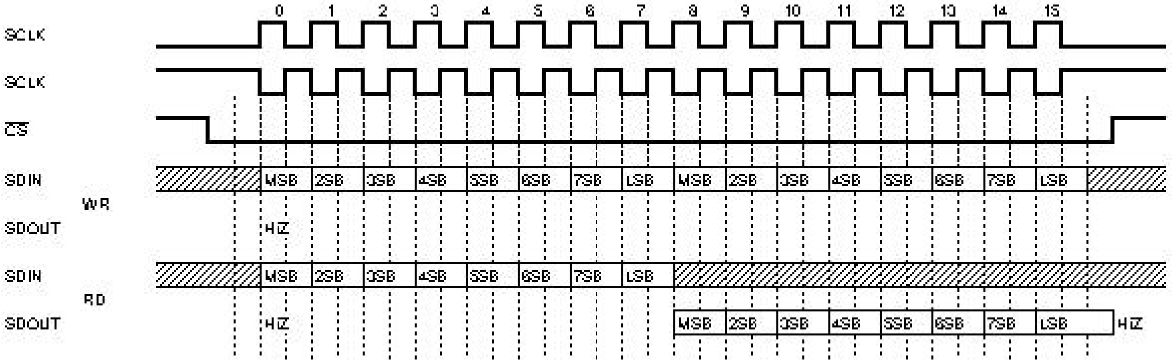
When serial interface is chosen, data from SDIN is latched into LSI synchronizing with SCLK. And data is output from SDOUT synchronizing with SCLK also.

ML2864 support four kind of timing for data input and output according to the condition below.

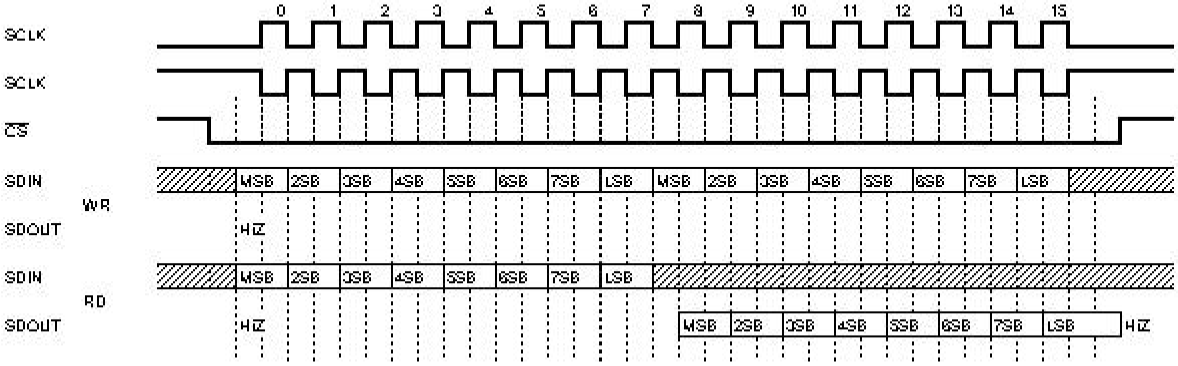
Please choose a suitable timing depending on CPU.

- Signal level of SCLK when CSB is changed
- Level of DIPH

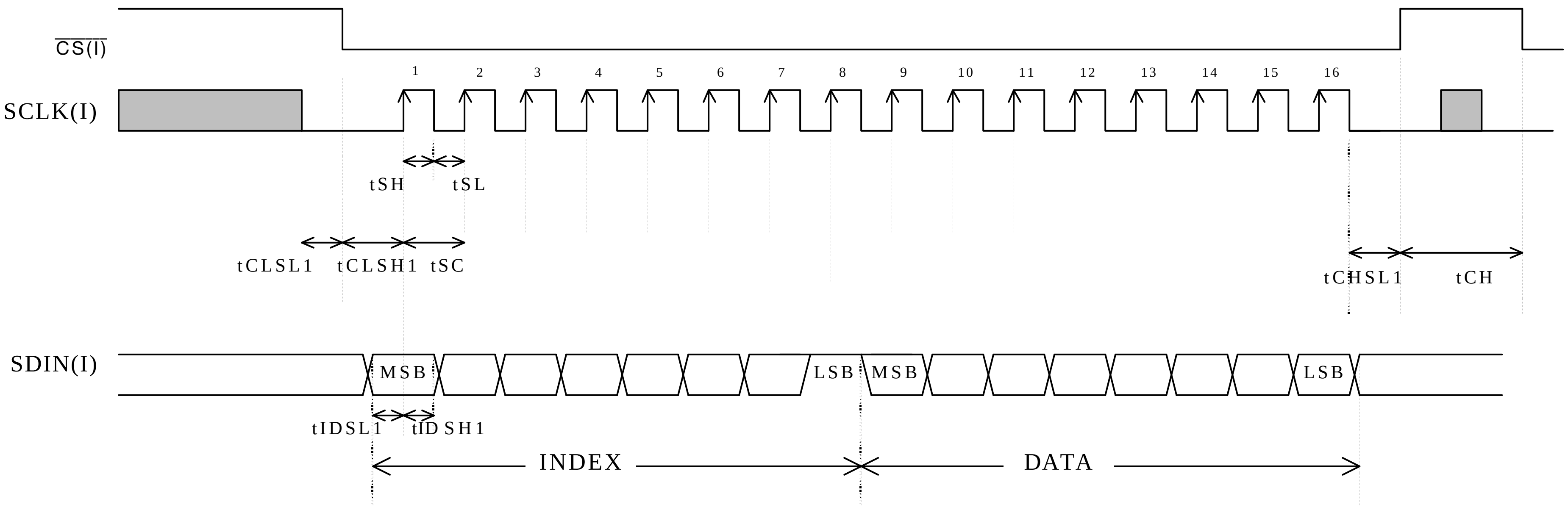
DIPH=0



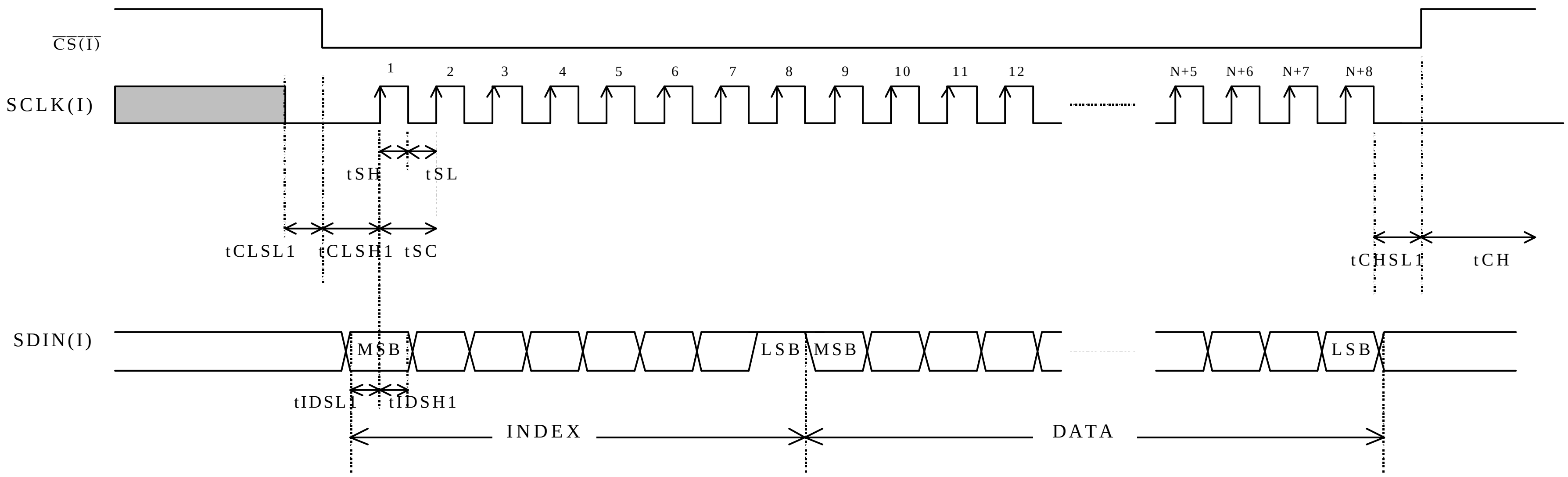
DIPH=1



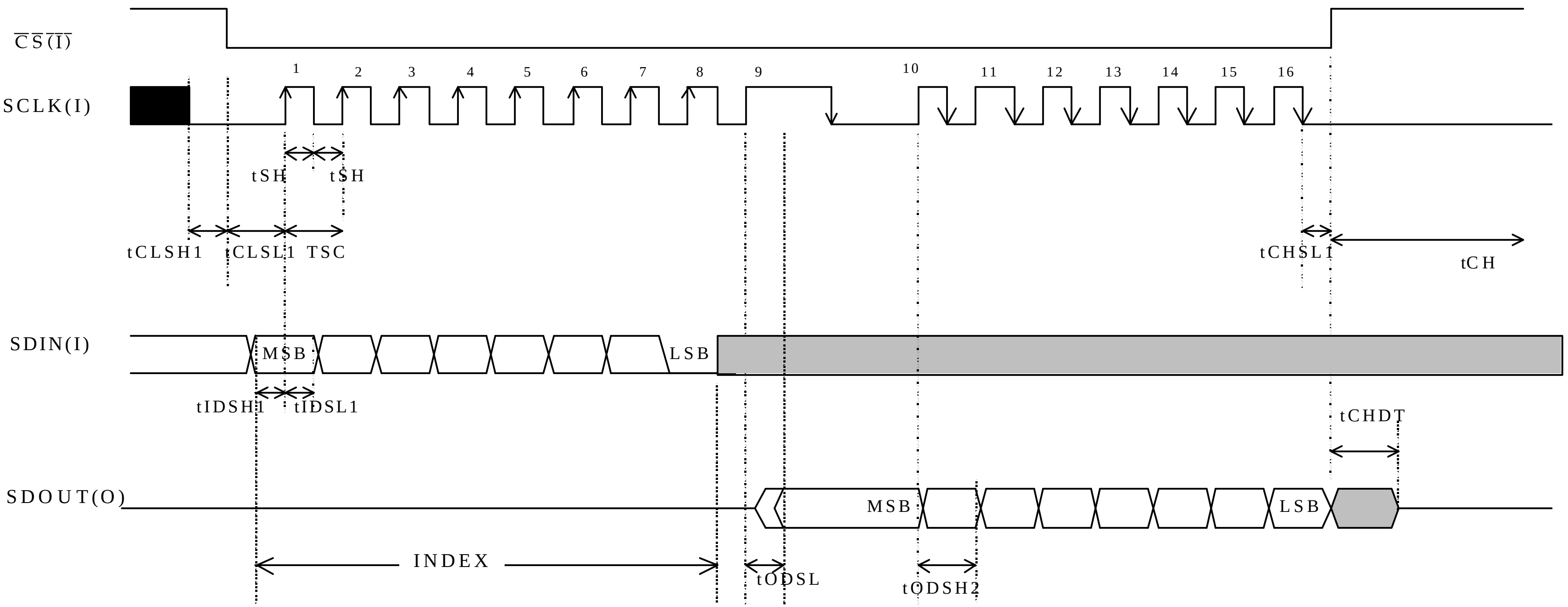
Data Write Timing1



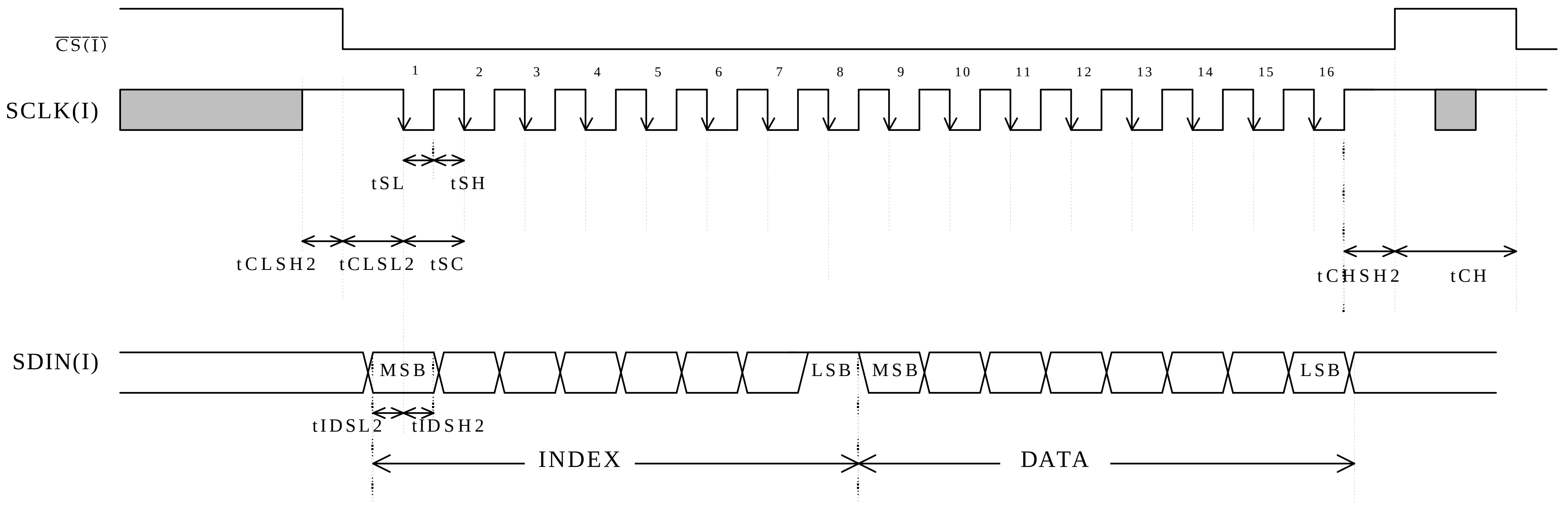
Data Write Timing to FIFO1



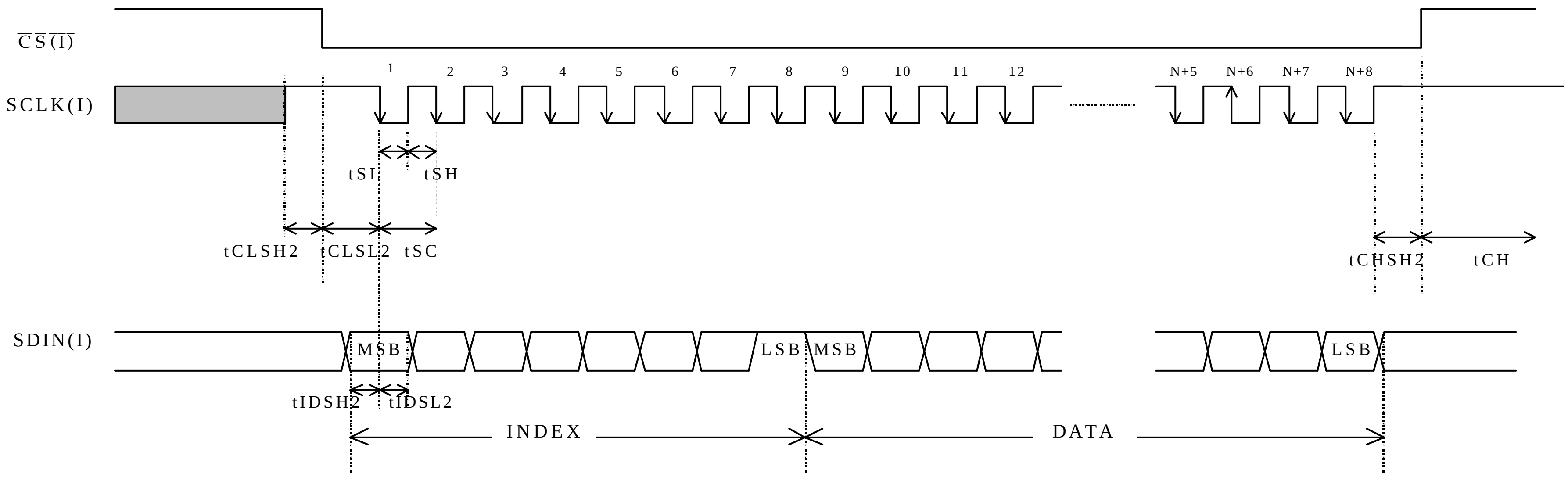
Data Read Timing1



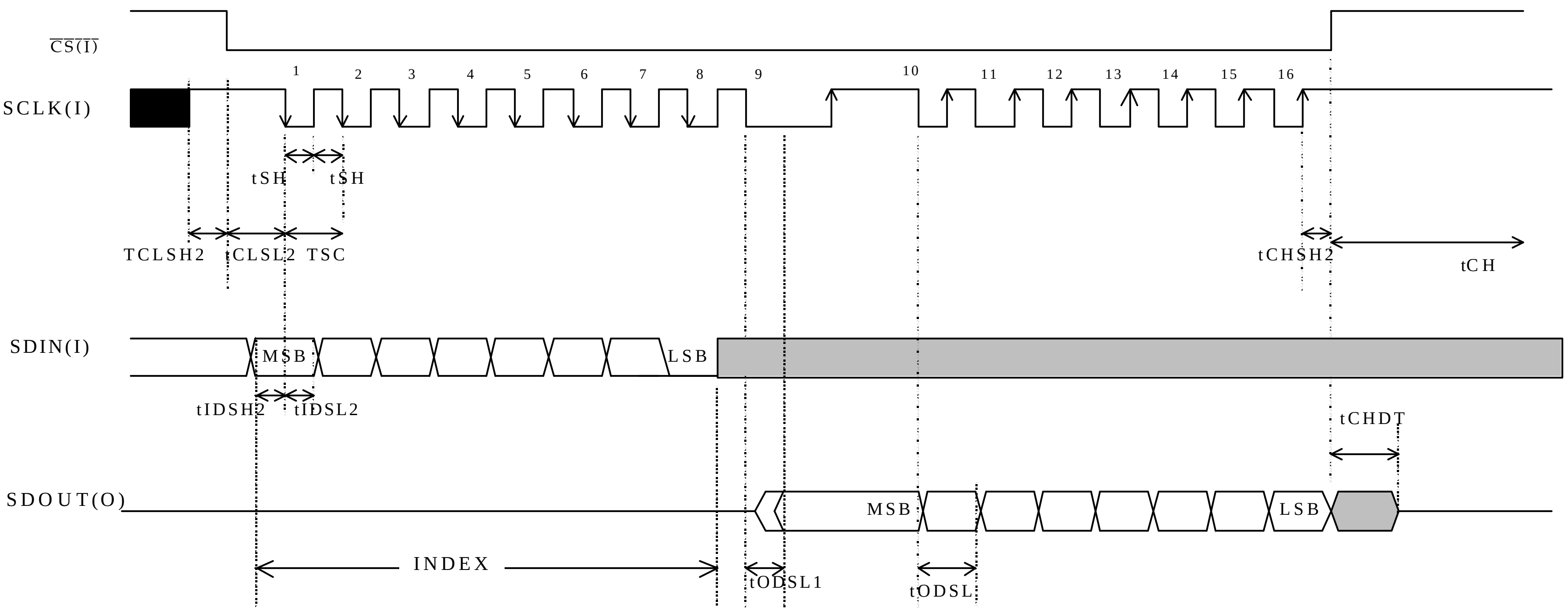
Data Write Timing2



Data Write Timing to FIFO2

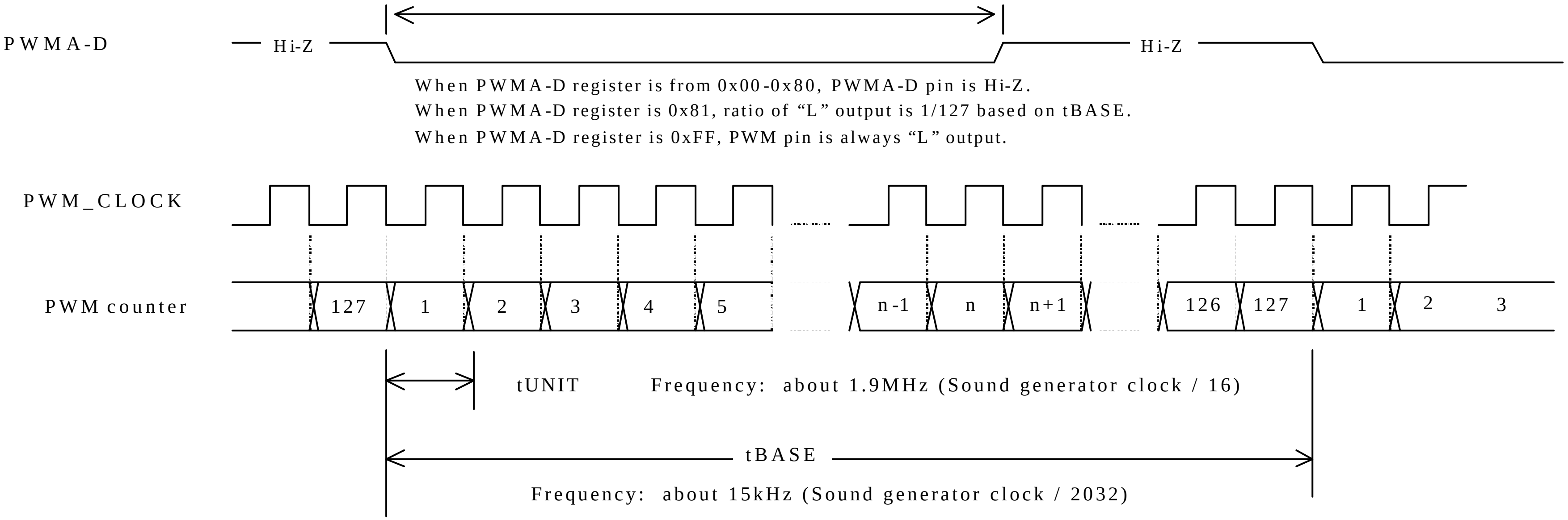


Data Read Timing2



Timing Chart of Functions

Timing chart of PWM output

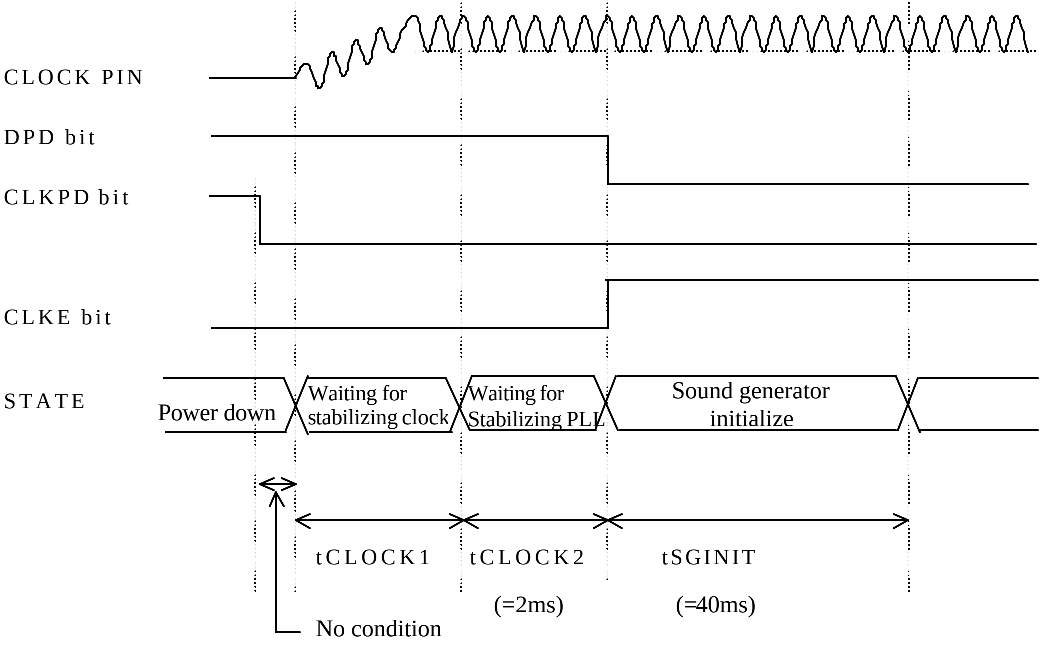


When PWMA-D register is from 0x00-0x80, PWMA-D pin is Hi-Z.
When PWMA-D register is 0x81, ratio of "L" output is 1/127 based on tBASE.
When PWMA-D register is 0xFF, PWM pin is always "L" output.

tUNIT Frequency: about 1.9MHz (Sound generator clock / 16)

tBASE Frequency: about 15kHz (Sound generator clock / 2032)

Supplying clock of small amplitude

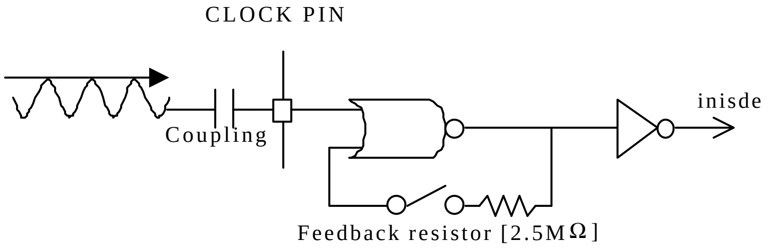


*1)During the "tSGINIT", an external CPU can access all the REGISTER in ML2870 except for ST bit and RCLR bit.

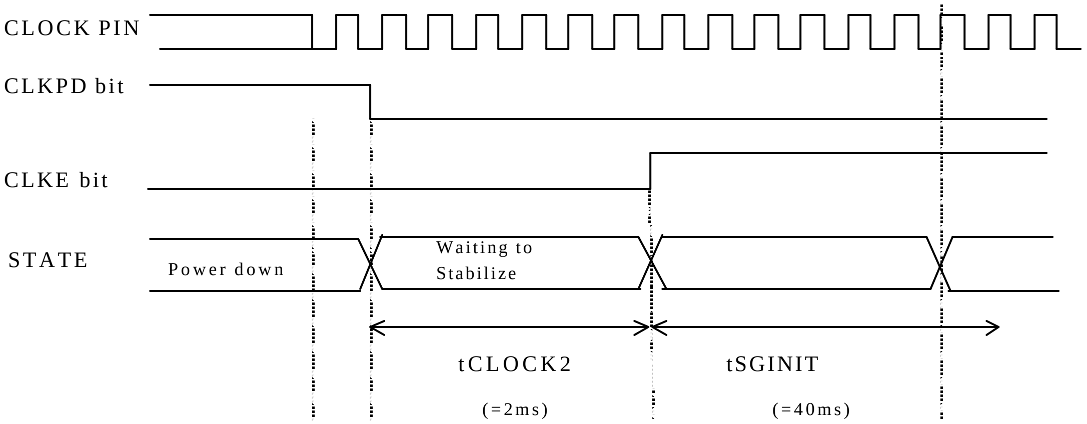
*2) ML2870 needs "tCLOCK1" for stabilizing signal before starting PLL operation.

*3) When ML2870 is supplied the clock of small amplitude, the value of capacitor for AC coupling determines "tCLOCK1" period.

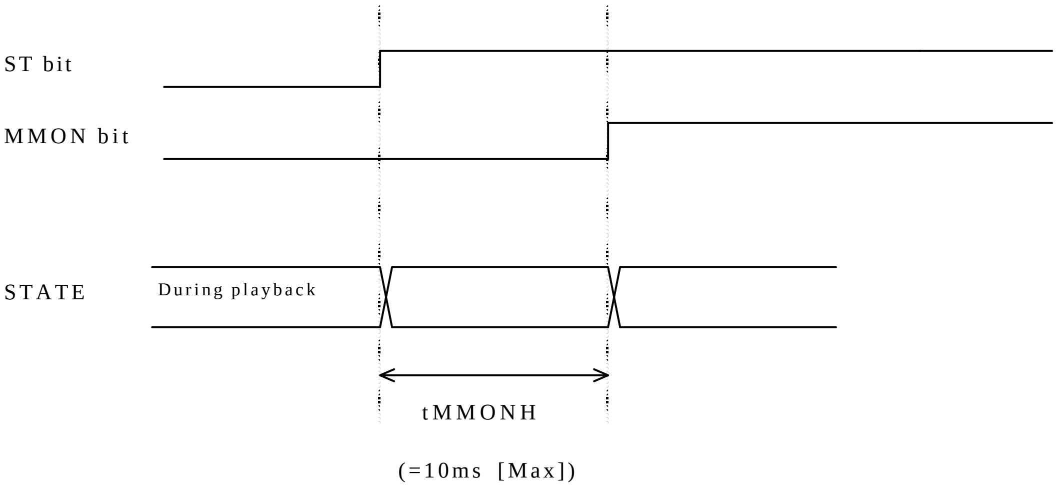
Capacitor	tCLOCK1 (MAX)
100pF	0.5ms
1000pF	5ms
0.01μF	50ms
0.1μF	500ms



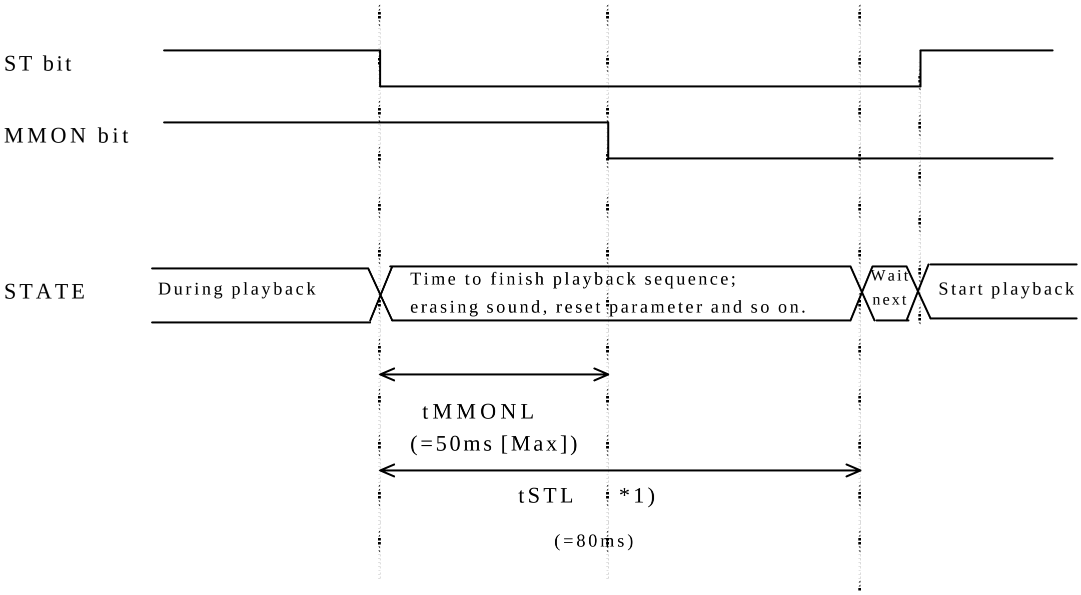
Supplying Clock of digital signal



Start Playback

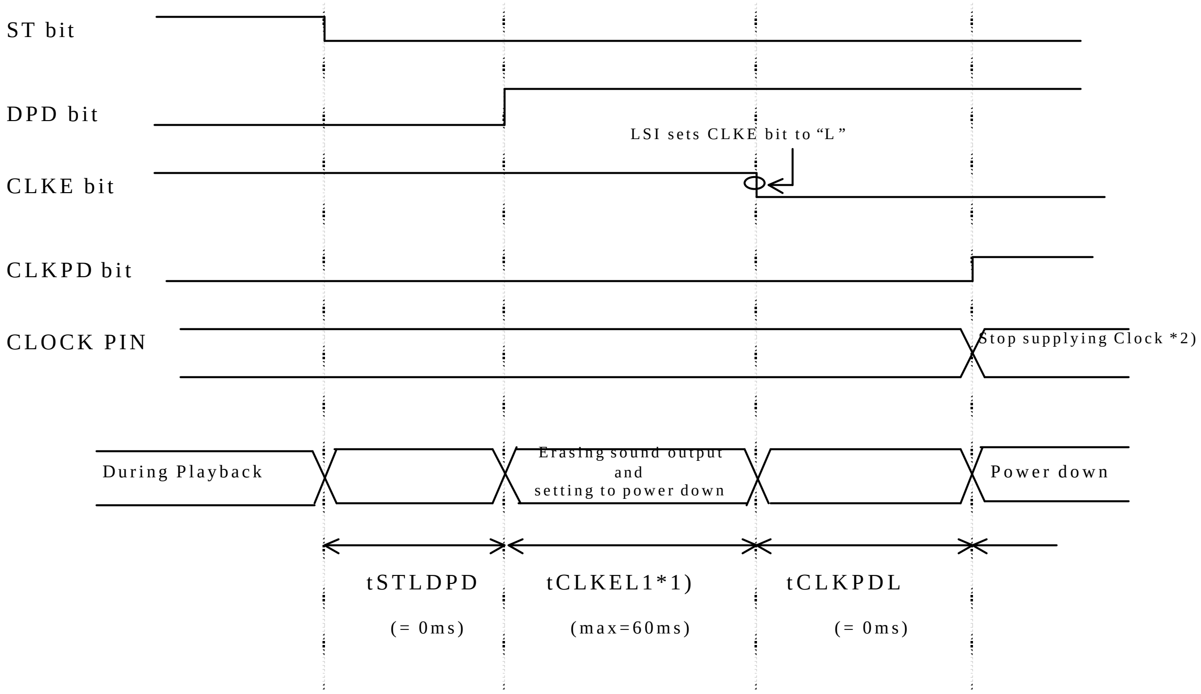


End of Playback and playback again



*1) When LSI is in tSTL state, external CPU can access all resister except for ST bit and RCCR bit.

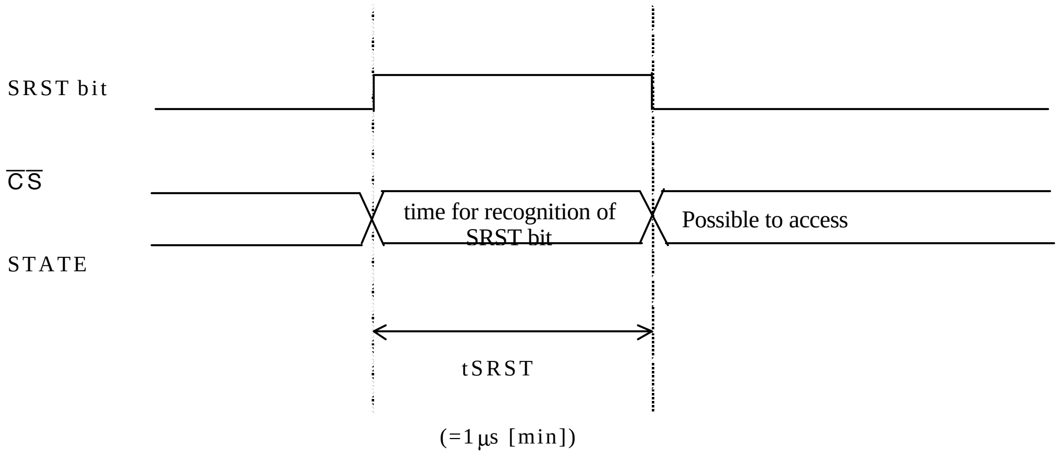
Power down sequence during Playback



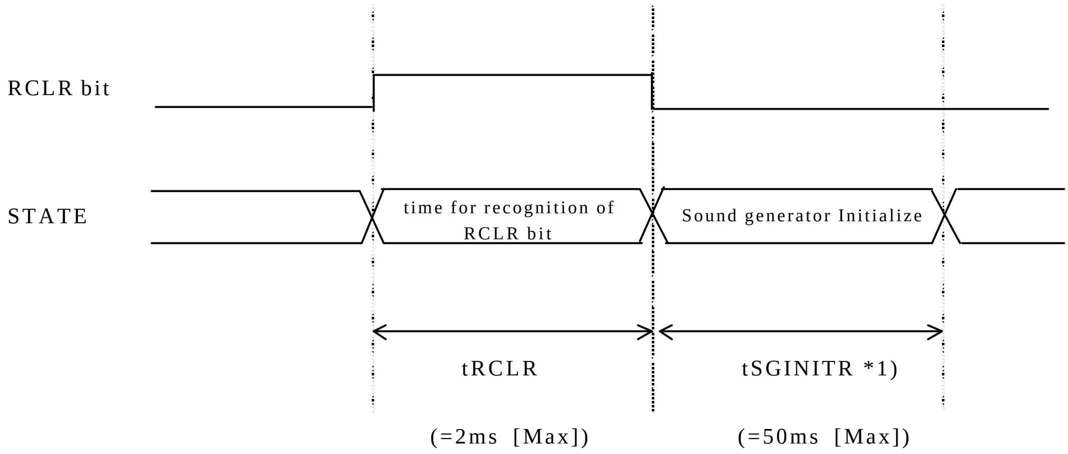
*1) Depending on the number of polyphony, tCLKEL1 is different in order to erase all sound naturally.

*2) Power down current consumption doesn't depend on the level of CLOCK PIN.

Software reset timing

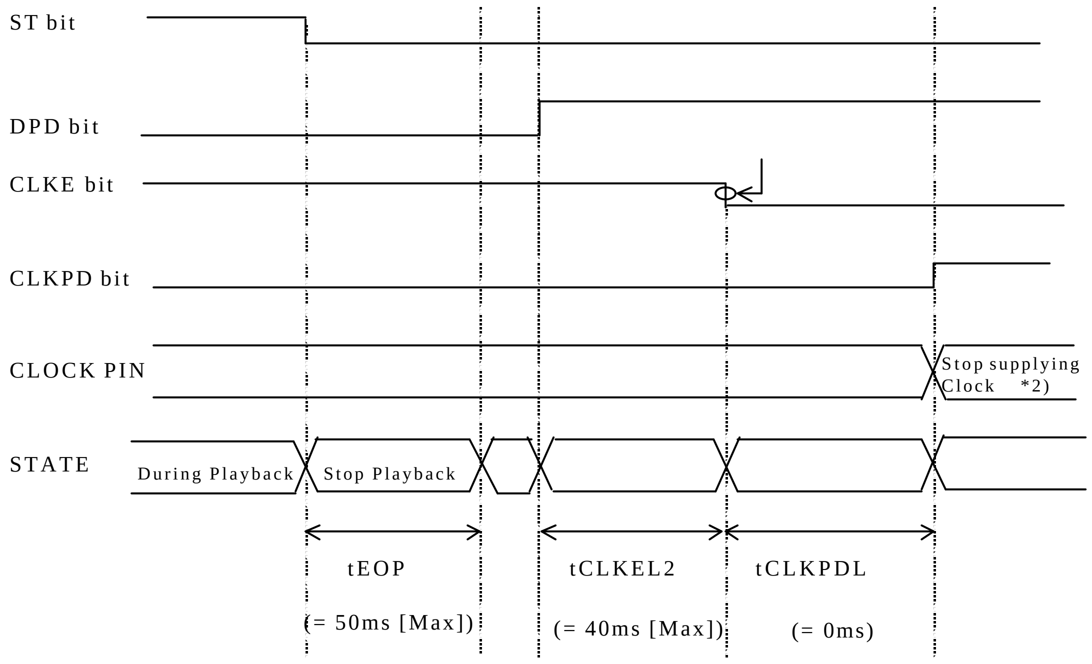


Register Clear timing

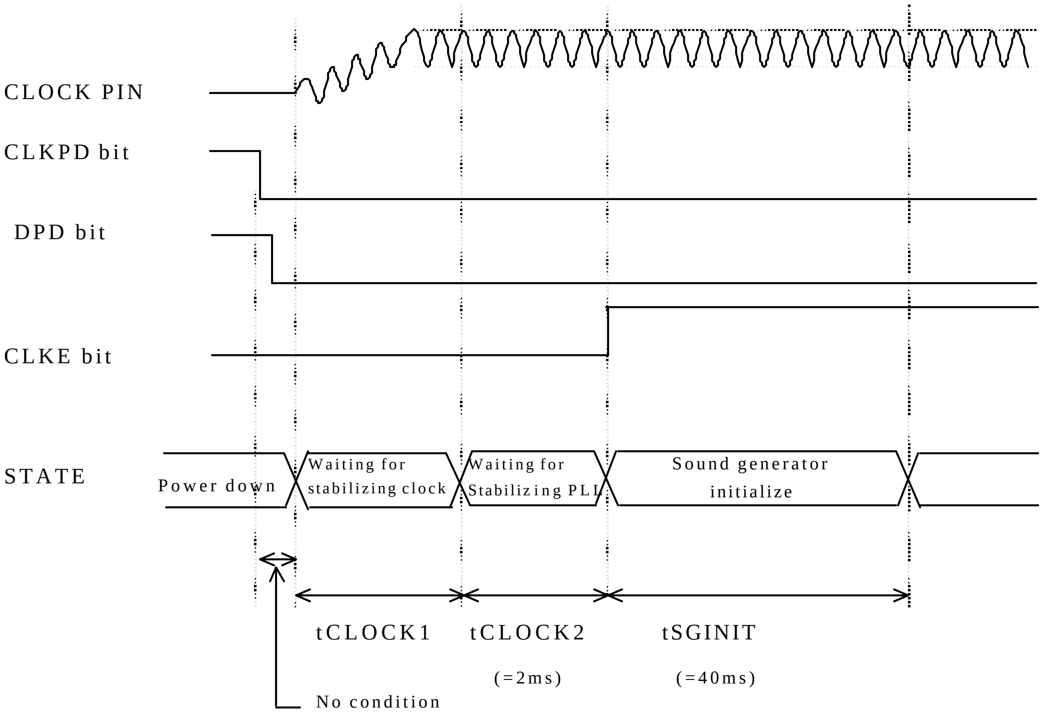


*1) When LSI is in “tSGINITR”, external CPU can access to register except for ST bit and RCLR bit.

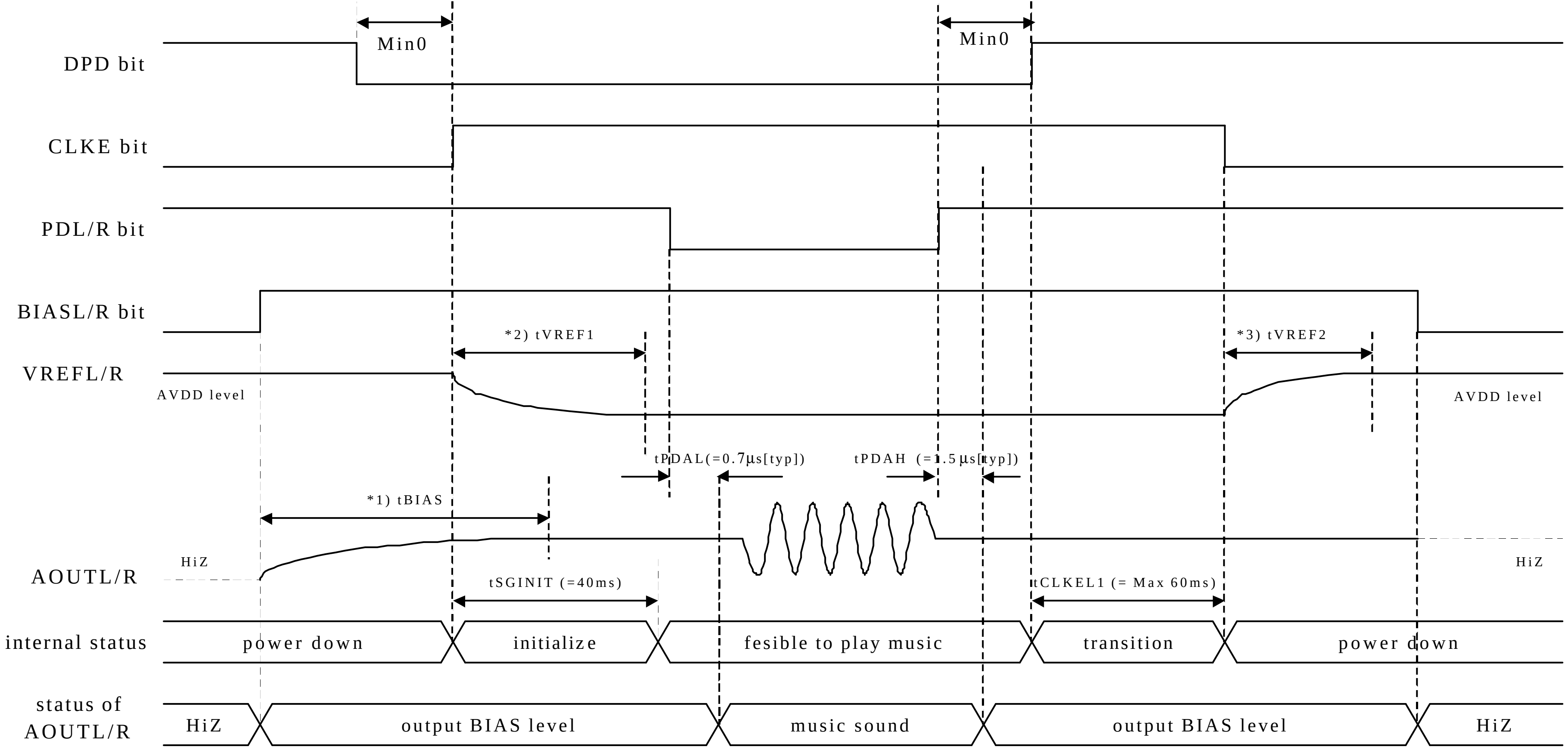
Power down sequence



Power up sequence (Reset Power Down)



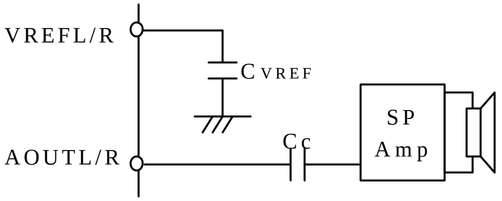
Timing chart of analog power down



*1) tBIAS(typ) = 2π x Cc x 300 x 10^3

*2) tVREF1(typ) = 2π x C_{VREF} x 13.5 x 10^3

*3) tVREF2(typ) = 2π x C_{VREF} x 31.6 x 10^3



POWER SUPPLY

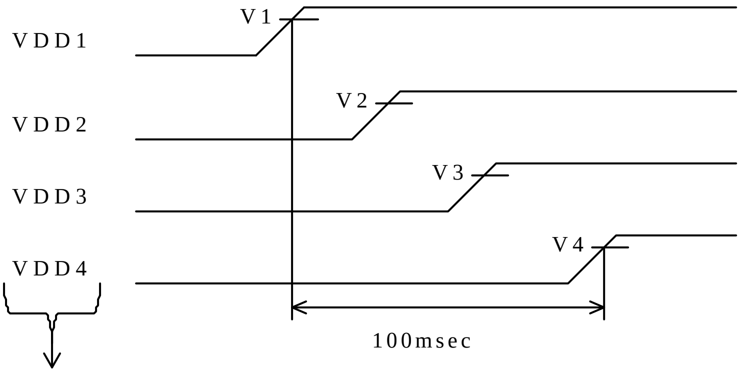
TIMING CHART FOR RAISING POWER SUPPLY

There are four kind of power supply in ML2870: VDDIO,DVDD,XTVDD and AVDD.

VDDIO is to supply only for bus interface. Voltage range is from 1.8V to DVDD.

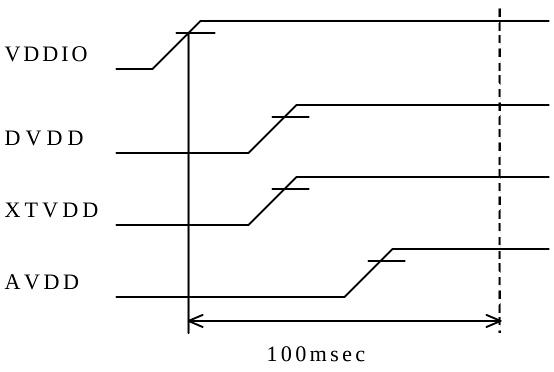
DVDD is for digital logic part. and XTVDD is only for oscillation part. DVDD and XTVDD are needed to supply by common source. When VDDIO is connected to same voltage as DVDD, or when CPU I/F is used as serial mode, DVDD and VDDIO have to be supplied by same source.

AVDD is for analog part. AVDD is able to separate from DVDD source. Also, the range of voltage is from 2.5V to 3.6V. Take care of timing to power on as showed at the following figure. It will cause Latch-up when the difference of time is longer than 100ms.



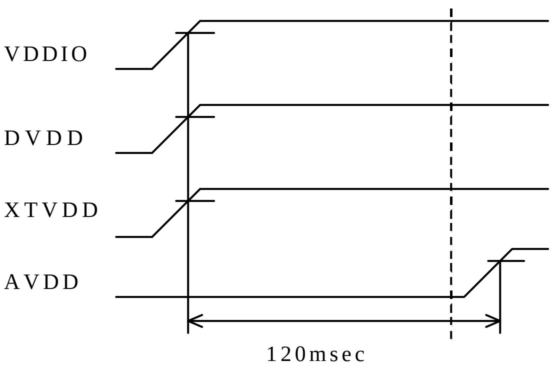
Any one of VDDs [VDDIO, DVDD, XTVDD, and AVDD]

[GOOD Example]



A current is supplied to the four VDD pins within 100ms. It is not important an order to power on.

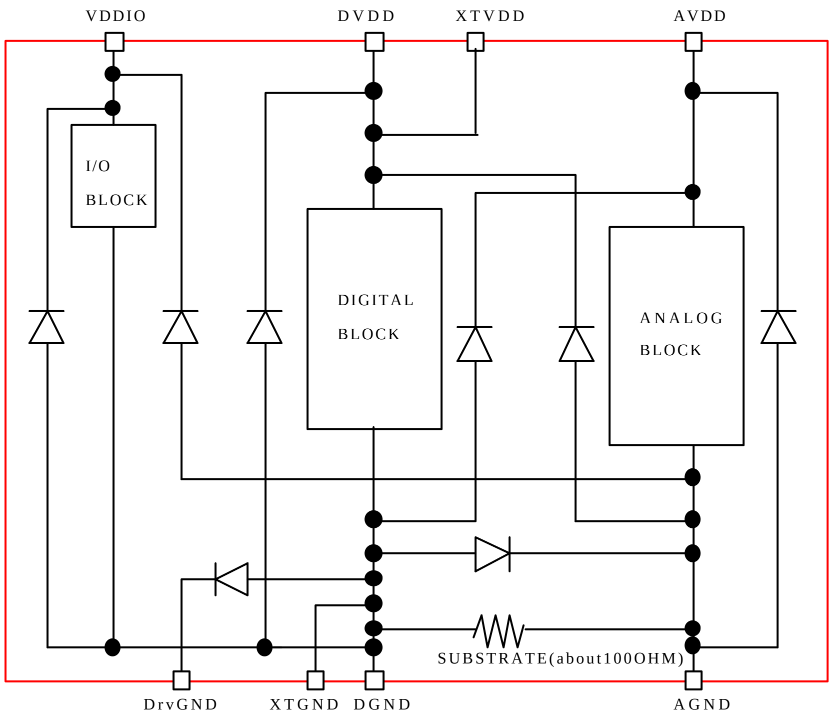
[NG Example]



Do not spend longer than 100ms to power on.

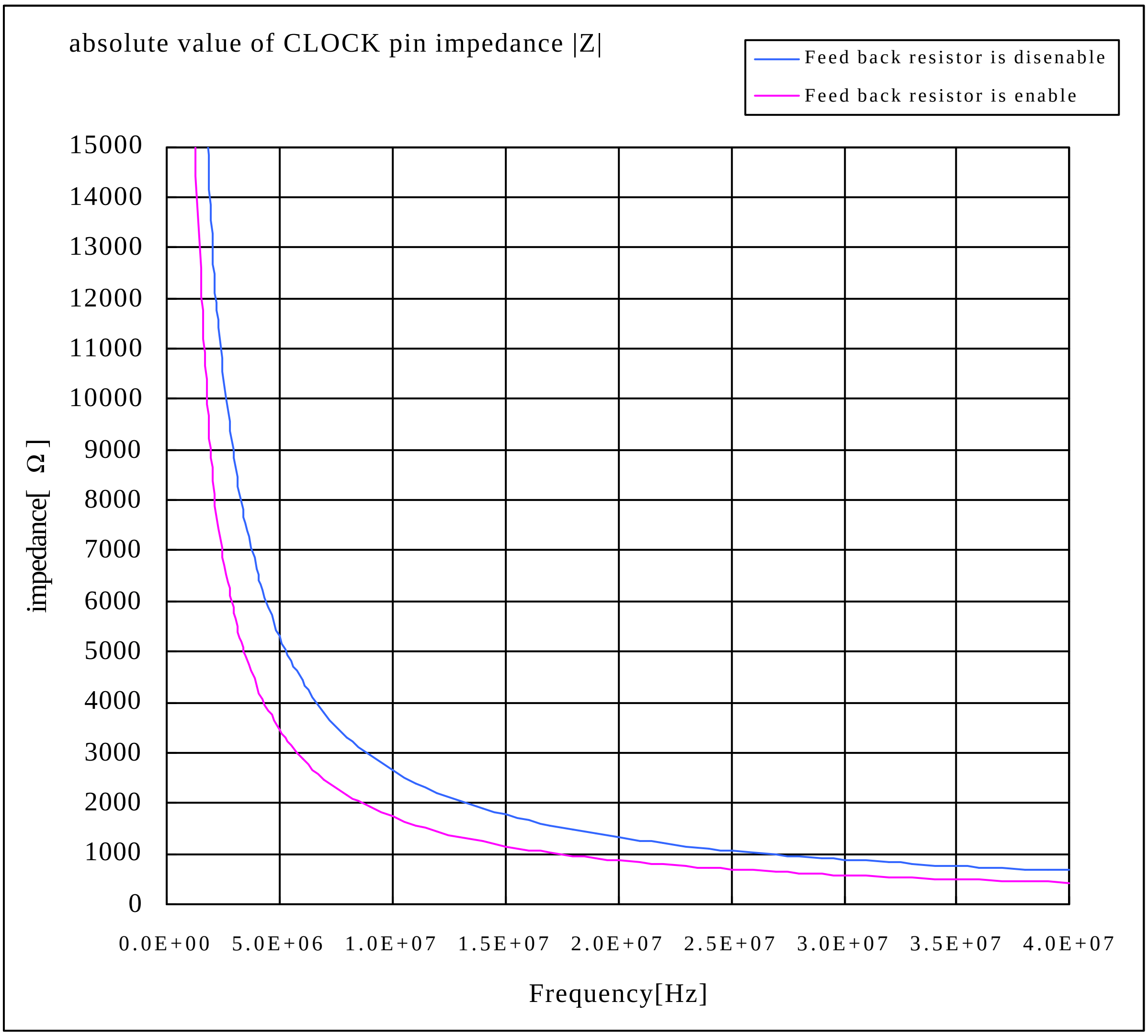
EQUIVALENT CIRCUIT

Following figure shows the equivalent circuit in part of power supply.

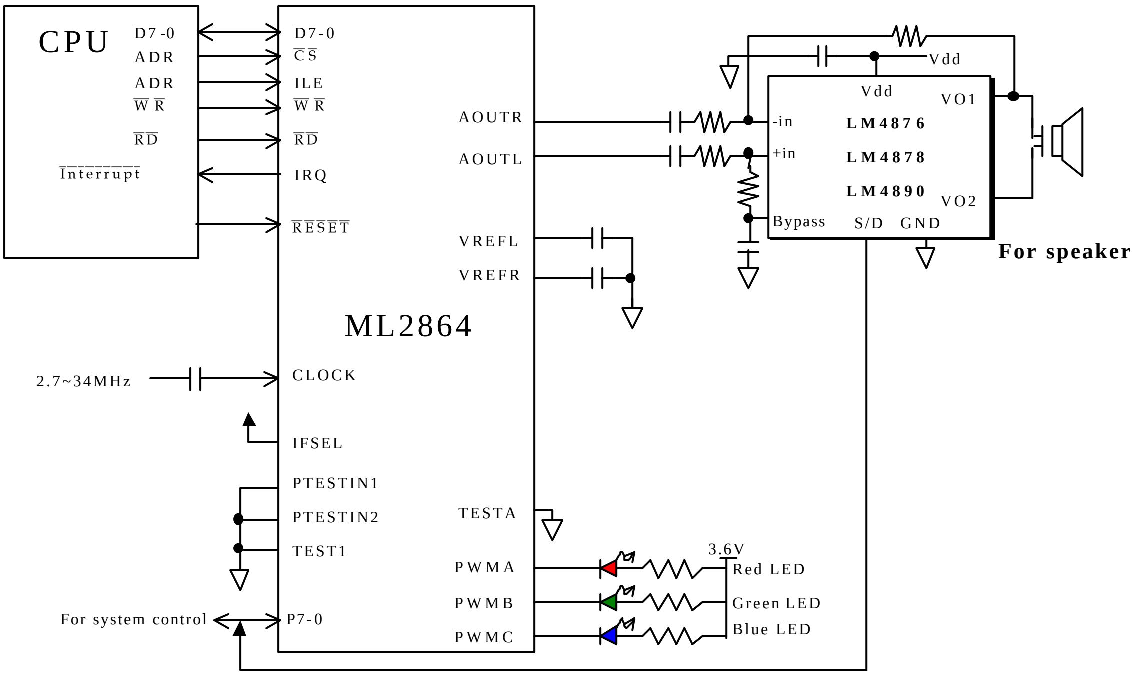


ABSOLUTE VALUE OF CLOCK PIN IMPEDANCE

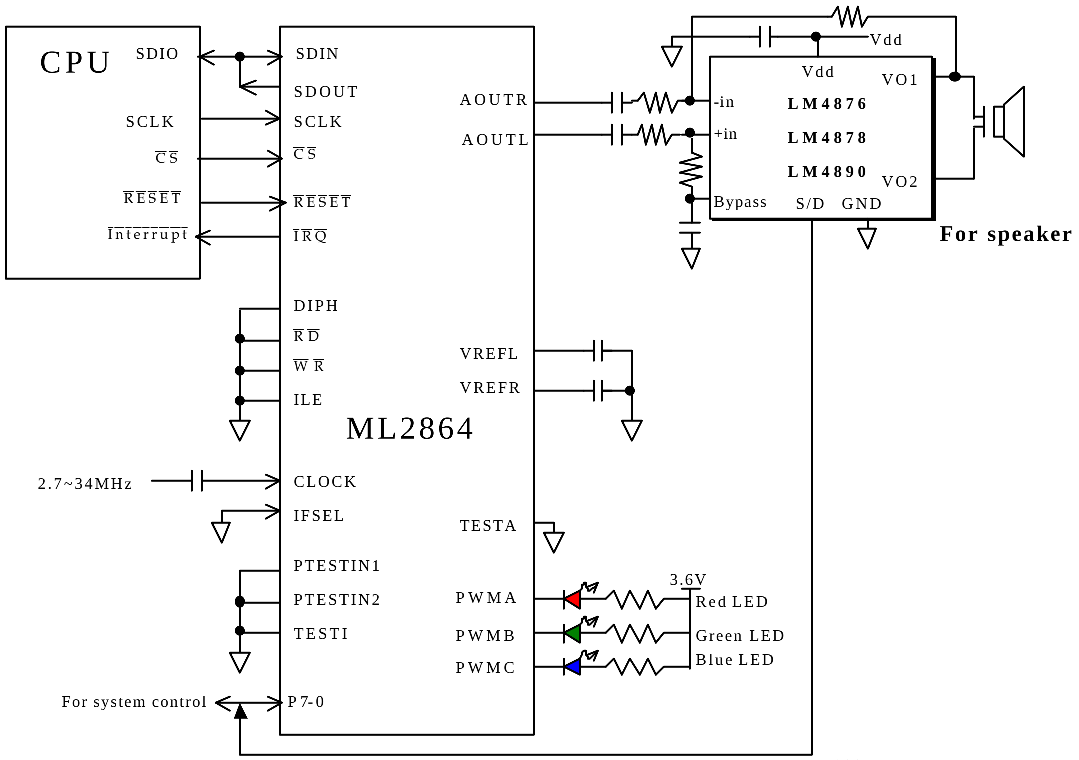
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
D7-0PIN floating capacitance	Cbus	-	-	12	18	pF
CLOCK pin impedance |Z| (FEED OFF: FEEDbit=0 or during power down)	Zclk1	3MHz	6.5	8.8	-	kΩ
		5MHz	4.0	5.3	-	kΩ
		10MHz	2.0	2.7	-	kΩ
		13MHz	-	2.1	-	kΩ
		20MHz	1.0	1.3	-	kΩ
		30MHz	0.65	0.88	-	kΩ
CLOCK pin impedance |Z| and during power on	Zclk2	3MHz	4.5	5.8	-	kΩ
		5MHz	2.5	3.5	-	kΩ
		10MHz	1.3	1.7	-	kΩ
		13MHz	-	1.30		kΩ
		20MHz	0.65	0.86	-	kΩ
		30MHz	0.45	0.58	-	kΩ

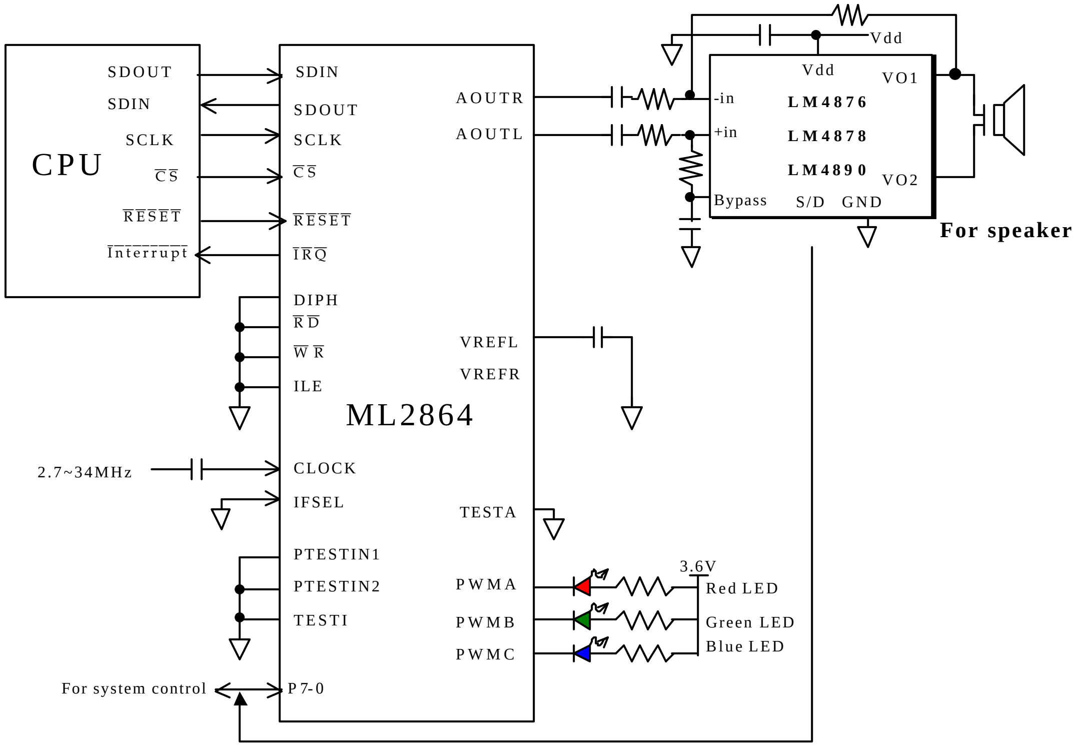


APPLICATION CIRCUIT EXAMPLE (BUS INTERFACE)



APPLICATION CIRCUIT EXAMPLE (SERIAL INTERFACE)





FUNCTIONAL DESCRIPTION OF THE REGISTERS

REGISTER MAP 1

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
	$01h	d07	d06	d05	d04	d03	d02	d01	d00	ADPCM FIFO
		0	0	0	0	0	0	0	0	ACOMP RAM
	$03h	d07	d06	d05	d04	d03	d02	d01	d00	Score FIFO
		0	0	0	0	0	0	0	0	
	$05h	d07	d06	d05	d04	d03	d02	d01	d00	Event FIFO
		0	0	0	0	0	0	0	0	
$06h		-	-	EFULL	SFULL	AFULL	EEMP	SEMP	AEMP	FIFO Status
		-	-	0	0	0	1	1	1	
$08h	$09h	-	-	-	-	RCLR	ECLR	SCLR	ACLR	CLR
		-	-	-	-	0	0	0	0	
LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$10h	$11h	PLL2	PLL1	PLL0	CK4	CK3	CK2	CK1	CK0	CLOCK
		0	0	0	0	0	0	0	0	-
$12h	$13h	Cent7	Cent6	Cent5	Cent4	Cent3	Cent2	Cent1	Cent0	Pitch Control
		0	0	0	0	0	0	0	0	
$14h	$15h	FEED	-	TMP4	TMP3	TMP2	TMP1	TMP0	Cent8	Pitch & Tempo Control
		0	-	0	0	0	0	0	0	
$16h	$17h	-	-	-	CLPD	CLKE			DPD	Power Down
		-	-	-	0	0	-	-	0	
$18h	$19h	-	S06	S05	S04	S03	S02	S01	S00	Master Clock Tuning
-		-	0	0	0	0	0	0	0	-
$1Ah	$1Bh	-	-	-	-	-	M2	M1	M0	MODE
		-	-	-	-	-	0	0	0	-
$1Eh	$1Fh	-	-	-	-	-	-	-	SRST	Soft Reset
		-	-	-	-	-	-	-	0	-

REGISTER MAP 2

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$20h	$21h	AIRQ7	AIRQ6	AIRQ5	AIRQ4	AIRQ3	AIRQ2	AIRQ1	AIRQ0	ADPCM Interrupt L
		0	0	0	0	0	0	0	0	-
$22h	$23h	-	-	-	-	-	-	-	AIRQ8	ADPCM Interrupt H
		-	-	-	-	-	-	-	0	-
$24h	$25h	-	SIRQ6	SIRQ5	SIRQ4	SIRQ3	SIRQ2	SIRQ1	SIRQ0	Score Interrupt
		-	0	0	0	0	0	0	0	-
$26h	$27h	-	-	-	-	EIRQ3	EIRQ2	EIRQ1	EIRQ0	Event Interrupt
		-	-	-	-	0	0	0	0	-
$28h	$29h	-	-	-	SYNCE	ISS	EIE	SIE	AIE	Interrupt Enable
		-	-	-	0	0	0	0	0	-
$2Ah	$2Bh	-	-	-	SYNC	ERR	ERQ	SRQ	ARQ	REQUEST
		-	-	-	0	0	0	0	0	-
$2Ch		-	-	-	MMON	AMON	-	-	-	STATUS
		-	-	-	0	0	-	-	-	-

Music & Voice Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$30h	$31h	-	-	-	-	-	-	PAUSE	ST	MUSIC START
		-	-	-	-	-	-	0	0	
$32h	$33h	-	-	-	-	-	-	MsyE	AST	ADPCM START
		-	-	-	-	-	-	0	0	
$34h	$35h	-	-	-	-	F3	F2	F1	F0	Fsamp
		-	-	-	-	0	0	0	0	
$36h	$37h	PL3	PL2	PL1	PL0	PR3	PR2	PR1	PR0	ADPCM PAN
		0	0	0	0	0	0	0	0	
$38h	$39h	-	-	-	ADVL4	ADVL3	ADVL2	ADVL1	ADVL0	Volume (ADPCM)
		-	-	-	0	0	0	0	0	

REGISTER MAP 3

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$40h	$41h	P7M 0	P6M 0	P5M 0	P4M 0	P3M 0	P2M 0	P1M 0	P0M 0	PORT MODE -
$42h	$43h	PI/O7 0	PI/O6 0	PI/O5 0	PI/O4 0	PI/O3 0	PI/O2 0	PI/O1 0	PI/O0 0	PORT I/O -
$44h	$45h	P7 1	P6 1	P5 1	P4 1	P3 1	P2 1	P1 1	P0 1	PORT -
$46h	$47h	- -	- -	WVM 0	WPM 0	WDM 0	WCM 0	WBM 0	WAM 0	PWM MODE -
$48h	$49h	WAE 0	WA6 0	WA5 0	WA4 0	WA3 0	WA2 0	WA1 0	WA0 0	PWMA -
$4Ah	$4Bh	WBE 0	WB6 0	WB5 0	WB4 0	WB3 0	WB2 0	WB1 0	WB0 0	PWMB -
$4Ch	$4Dh	WCE 0	WC6 0	WC5 0	WC4 0	WC3 0	WC2 0	WC1 0	WC0 0	PWMC -
$4Eh	$4Fh	WDE 0	WD6 0	WD5 0	WD4 0	WD3 0	WD2 0	WD1 0	WD0 0	PWMD -
$50h	$51h	WPE 0	WP6 0	WP5 0	WP4 0	WP3 0	WP2 0	WP1 0	WP0 0	Panel -
$52h	$53h	WVE 0	WV6 0	WV5 0	WV4 0	WV3 0	WV2 0	WV1 0	WV0 0	Vib -
$54h	$55h	$\overline{\text{PUP7}}$ 0	$\overline{\text{PUP6}}$ 0	$\overline{\text{PUP5}}$ 0	$\overline{\text{PUP4}}$ 0	$\overline{\text{PUP3}}$ 0	$\overline{\text{PUP2}}$ 0	$\overline{\text{PUP1}}$ 0	$\overline{\text{PUP0}}$ 0	$\overline{\text{Pull-up}}$ (Port) -
$56h	$57h	$\overline{\text{P7}}$/PZ 0	$\overline{\text{P6}}$/PY 0	$\overline{\text{P5}}$/PV 0	$\overline{\text{P4}}$/PP 0	$\overline{\text{P3}}$/PD 0	$\overline{\text{P2}}$/PC 0	$\overline{\text{P1}}$/PB 0	$\overline{\text{P0}}$/PA 0	PWM output select -

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$62h	$63h	VR3 0	VR2 0	VR1 0	VR0 0	VL3 0	VL2 0	VL1 0	VL0 0	Audio Volume -
$66h	$67h	BIASR 0	PDR 1	ENL2R 0	ENR2R 1	BIASL 0	PDL 1	ENR2L 0	ENL2L 1	Analog Power Down -
$68h	$69h							AORINV 0	AOLINV 0	AOUT Invert (for BTL mode)

DIFFERENCE BETWEEN HARDWARE RESET AND SOFTWARE RESET

There are four way for reset.

1. $\overline{\text{RESET}}$ pin is “L”.
2. SRST, ”software reset”, register is “H”.
3. DPD, which selects power down state of all functions, is “H”.
4. RCLR, “register clear”, register is “H”.

The following table shows the difference between each function.

Table 6: RESET Functions

Registers/ Functions	Detail	RESET pin	SRST	DPD bit = 1	RCLR
Registers	ADPCM FIFO	EMPTY	EMPTY	EMPTY	EMPTY
	SCORE FIFO	EMPTY	EMPTY	EMPTY	EMPTY
	EVENT FIFO	EMPTY	EMPTY	EMPTY	EMPTY
	CLR	Reset	Reset	No change	No change
	CLOCK	Reset	No change	No change	No change
	Pitch control	Reset	No change	No change	No change
	Pitch & tempo	Reset	No change	No change	No change
	Power down (CLKE bit)	Reset	Reset	Reset	No change
	Power down (Except for CLKE bit)	Reset	Reset	No change	No change
	Master clock tuning	Reset	No change	No change	No change
	MODE	Reset	Reset	No change	Reset
	Soft reset	Reset	No change	No change	No change
	ADPCM interrupt	Reset	Reset	No change	Reset
	Score interrupt	Reset	Reset	No change	Reset
	Event interrupt	Reset	Reset	No change	Reset
	Interrupt Enable (Except for ISS bit)	Reset	Reset	No change	Reset
	Interrupt Enable (ISS bit)	Reset	Reset	No change	No change
	MUSIC START	Reset	Reset	No change	Reset
	ADPCM START	Reset	Reset	No change	Reset
	Fsamp	Reset	Reset	No change	Reset
	APAN	Reset	Reset	No change	No change
	Volume (ADPCM)	Reset	Reset	No change	No change
	Port mode	Reset	Reset	No change	No change
	Port I/O	Reset	Reset	No change	No change
	Port	Reset	Reset	No change	No change
	PWM mode	Reset	Reset	No change	No change
	PWM of LEDA	Reset	Reset	No change	No change
	PWM of LEDB	Reset	Reset	No change	No change
	PWM of LEDC	Reset	Reset	No change	No change
	PWM of Panel	Reset	Reset	No change	No change
	PWM of VIB	Reset	Reset	No change	No change
	$\overline{\text{PULLUP}}$	Reset	Reset	No change	No change
	PWM output select	Reset	Reset	No change	No change
	Analog Volume	Reset	Reset	No change	No change
	Analog Power Down	Reset	Reset	No change	No change
	AOUT invert	Reset	Reset	No change	No change
Functions	Sound generator	Reset	Reset	Reset	Reset
	ADPCM	Reset	Reset	Reset	Reset

	PWM	Reset	Reset	Reset	No change

DETAILED DESCRIPTION OF THE REGISTERS

ADPCM FIFO and Accompaniment Register (Read : inhibit / Write : $01h)

This register accommodates ADPCM data or accompaniments. When you replay ADPCM, MODE register is set to “00h”.

<ADPCM FIFO mode>

As ADPCM is replayed, the data stored in the FIFO is ADPCM processed. The LSI outputs a data request signal from the ARQ register when the data in the ADPCM FIFO lowers to the threshold pre-defined by the AIRQ8-0 bits. Write the next ADPCM data when the data request signal is output from the ARQ register.

<Accompaniments Register>

The function of this mode is not disclosed.

Score FIFO (Read : inhibit / Write : $03h)

This SCORE register accommodates music data. Data entered to this register is being loaded and stored into the ML2870 internal Score FIFO.

ML2870 can play music by means of three score formats. ML2870 recognizes musical score formats by the first 4 bytes in the score data after ST bit is set to “H”.

Table 7: Relation between Format and Header Data

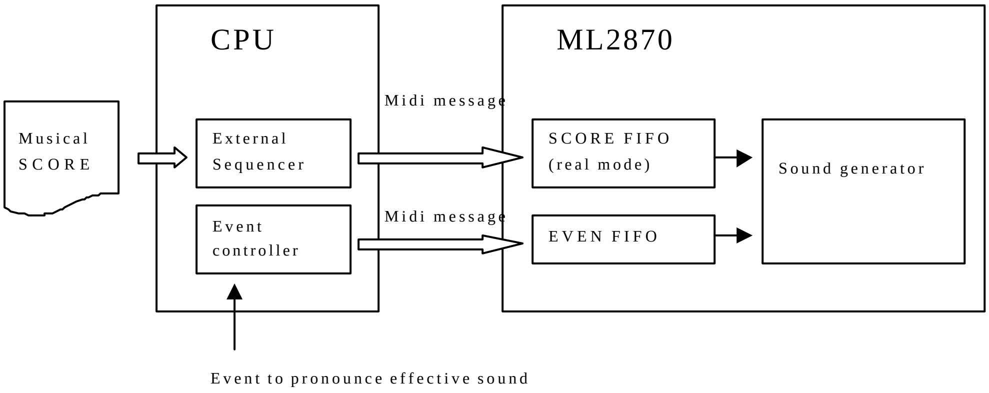
Format	Header
Real time MIDI events	‘real’
MCDF	‘MCDF’
SMF format 0 under some condition	‘MThd’

< Real Time MIDI Events Mode>

Real time MIDI events are shown by the MIDI implementation chart.

The score FIFO which is for real time MIDI events, is suitable to the following configuration.

It is easy to control by two kinds of controllers, such as external sequencer and event controller.



< MCDF >

After the customer agrees to an NDA, the MCDF document will be disclosed by OKI

< SMF format 0 with some condition >

SMF is standard MIDI File format. SMF specification are available at MMA. Oki supports a software for playback SMF 0 and SMF1.

EVENT FIFO (Read : inhibit / Write : $05h)

This Event register accommodates MIDI data. Data entered to this register is being loaded and stored into the ML2870 internal Event FIFO for MIDI.

The available data for the event FIFO is shown by the MIDI implementation chart.

Because the EVENT FIFO does not require timer data, it is possible to pronounce the musical note soon after data input.

FIFO status (Read $06h : / Write : inhibit)

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$06h		-	-	EFULL	SFULL	AFULL	EEMP	SEMP	AEMP	FIFO status
		-	-	0	0	0	1	1	1	

The FIFO status register outputs the empty flag and the full flag of each FIFO.

AEMP is the empty flag of the ADPCM FIFO. When the ADPCM FIFO is empty, AEMP is “1”. When data is input to the ADPCM FIFO, AEMP is “0”.

SEMP is the empty flag of the SCORE FIFO. When the SCORE FIFO is empty, SEMP is “1”. When data is input to the SCORE FIFO, SEMP is “0”.

EEMP is the empty flag of the EVENT FIFO. When the EVENT FIFO is empty, EEMP is “1”. When data is input to the EVENT FIFO, EEMP is “0”.

AFULL is the full flag of the ADPCM FIFO. When the ADPCM FIFO is full, AFULL is “1”. When data can be written to the ADPCM FIFO, AFULL is “0”.

SFULL is the full flag of the SCORE FIFO. When the SCORE FIFO is full, SFULL is “1”. When data can be written to the SCORE FIFO, SFULL is “0”.

EFULL is the full flag of the EVENT FIFO. When the EVENT FIFO is full, EFULL is “1”. When data can be written to the EVENT FIFO, EFULL is “0”.

CLR Register (Read $08h : / Write : $09h)

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$08h	$09h	- -	- -	- -	- -	RCLR 0	ECLR 0	SCLR 0	ACLR 0	CLR

The CLR Register clears each FIFO.

ADPCM FIFO is cleared upon setting ACLR to “1”.

SCORE FIFO is cleared upon setting SCLR to “1”.

EVENT FIFO is cleared upon setting ECLR to “1”.

When set RCLR bit to “1”, prescribed register which is shown by the chapter of “Difference Between Hardware Reset and Software Reset” is cleared.

CLOCK (Read $10h : / Write : $11h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$10h	$11h	PLL2 0	PLL1 0	PLL0 0	CK4 0	CK3 0	CK2 0	CK1 0	CK0 0	CLOCK -

The clock register determines the sound generator clock as submultiples of the master clock. CK4-0 bits set the division ratio of the master clock to the PLL. The PLL then multiplies that clock by the times which is corresponded to PLL bits, thus generating the sound generator clock that should range between 27 and 34 MHz..

PLL2-0 bits indicate the multiplication of clock by PLL operation.

The values for this register are shown in the chapter “Master clock frequency and clock register” in the application note.

Table 8

Value (CK4-0)	Divided Ratio	Value (CK4-0)	Divided Ratio
00H	1	0AH	11
01H	2	0BH	12
02H	3	0CH	13
03H	4	0DH	14
04H	5	0EH	15
05H	6	0FH	16
06H	7	10H	17
07H	8	11H	18
08H	9	12H	19
09H	10	13H	20
		14H-1FH	N/A

Table 9

Value (PLL2-0)	Times by PLL	Value (PLL2-0)	Times by PLL
0h	Inhibit (Not use PLL)	4h	16
1h	10	5h	18
2h	12	6h	20
3h	14	7h	20

Pitch control (Read $12h and : / Write : $13h)

LSI Control Register										
INDEX		b07	b06	b05	b04	B03	b02	b01	b00	NOTE
R	W	(Initial)								
$12h	$13h	Cent7 0	Cent6 0	Cent5 0	Cent4 0	Cent3 0	Cent2 0	Cent1 0	Cent0 0	Pitch Control

Pitch control register corrects the musical pitch according to the sound generator clock frequency. The values for this register is shown by the “Master clock frequency and clock register” in the application note.

Tempo Control (Read $14h : / Write : $15h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$14h	$15h	FEED 0	- -	TMP4 0	TMP3 0	TMP2 0	TMP1 0	TMP0 0	Cent8 0	Pitch & Tempo Control

The tempo register corrects the musical tempo according to the sound generator clock frequency. The values for this register are shown in the "Master clock frequency and clock register" in the application note.

TMP4 bit and Cent 8 bit are sign bit for correct tempo. When TMP4 bit and Cent8 bit is "1", value is minus. When TMP4 bit and Cent8 bit is "0", value is plus.

TMP3-0 bit is abstract value of tempo correct.

Table 10

Value (TMP4-0)		Corrected value	Value (TMP4-0)		Corrected value
15	0b01111	15%	-1	0b10001	-1%
14	0b01110	14%	-2	0b10010	-2%
13	0b01101	13%	-3	0b10011	-3%
12	0b01100	12%	-4	0b10100	-4%
11	0b01011	11%	-5	0b10101	-5%
10	0b01010	10%	-6	0b10110	-6%
9	0b01001	9%	-7	0b10111	-7%
8	0b01000	8%	-8	0b11000	-8%
7	0b00111	7%	-9	0b11001	-9%
6	0b00110	6%	-10	0b11010	-10%
5	0b00101	5%	-11	0b11011	-11%
4	0b00100	4%	-12	0b11100	-12%
3	0b00011	3%	-13	0b11101	-13%
2	0b00010	2%	-14	0b11110	-14%
1	0b00001	1%	-15	0b11111	-15%
0	0b000000 0b10000	No correct			

The FEED bit switches feedback resistor on clock pin ON or OFF.

Feedback resistance is effective at "1." Feedback resistance "1" inputs small amplitude clock.

Table 11

	Data	Description
FEED bit	0	The feedback resistor is not used
	1	The feedback register is used.

Power Down (Read $16h : / Write : $17h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$16h	$17h	- -	- -	- -	CLPD 0	CLKE 0	-	-	DPD 0	Power Down

The power down register selects the power down states of each block. Each bit is assigned to the power down signal of each respective block.

LSI will be in a power down state completely on the condition: CLPD bit is "1", CLKE bit is "0" and DPD bit is "1".

The state after system reset is not in power down mode. Please proceed power-on sequence and power-down sequence.

The DPD bit sets the power down state of the ADPCM and sound generator blocks.

The CLKE bit enables input of the sound generator clock.

The CLPD bit sets the power down state of the oscillation block.

Just for a reference, the figure below shows the internal operation.

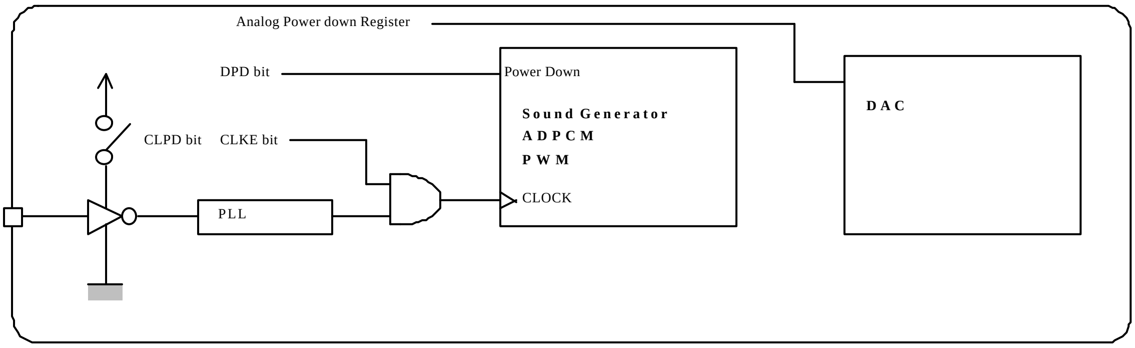
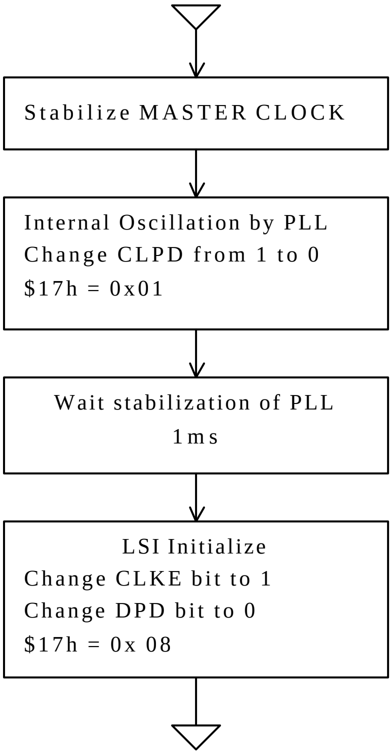


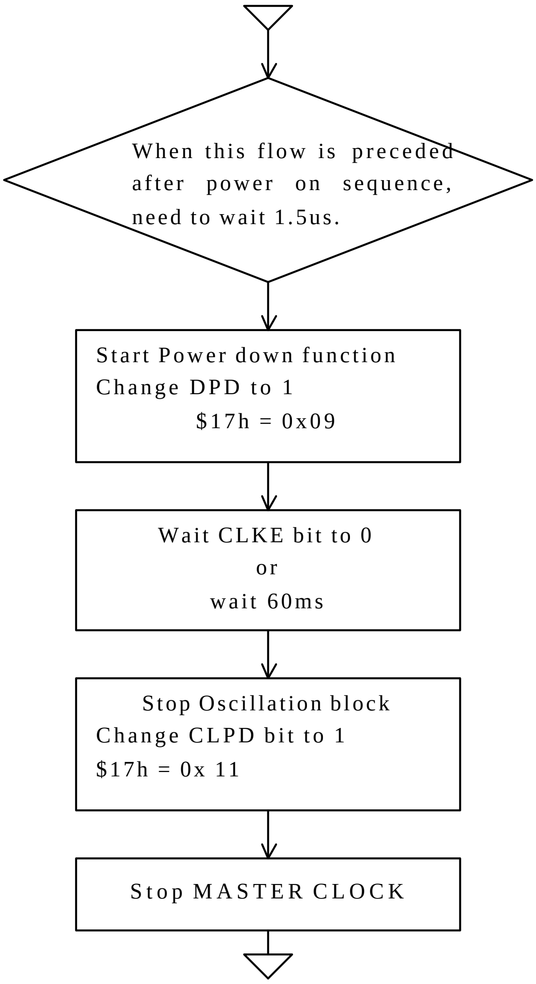
Table 12

	Data	Description
DPD bit	0	Ready.
	1	Power down state.
CLKE bit	0	No clock supply to the LSI's internal circuit. (i.e. waiting for the clock to stabilize.)
	1	Clock supply to the LSI's internal circuit. (i.e. the clock is stabilized.)
CLPD bit	0	Ready.
	1	Power down state.

Flowchart for Power on



Flow Chart for Power Down



Master Clock Tuning (Read $18h : / Write : $19h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$18h	$19h	-	S06	S05	S04	S03	S02	S01	S00	Master Clock Tuning
-		-	0	0	0	0	0	0	0	-

The master clock tuning register splits an audio clock into submultiples of the sound generator clock. The values for this register are shown in “Master clock frequency and clock register” in the application note..

MODE (Read $1Ah : / Write : $1Bh)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$1Ah	$1Bh	-	-	-	-	-	M2	M1	M0	MODE
		-	-	-	-	-	0	0	0	-

The mode register is fixed to “0”. Do not change to any other value.

Soft Reset (Read $1Eh : / Write : $1Fh)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$1Eh	$1Fh	- -	- -	- -	- -	- -	- -	- -	SRST 0	Soft Reset -

The soft reset register resets all blocks in the ML2870. The LSI initializes, when the SRST bit is “H”. The SRST bit is “L” while the ML2870 is active.

ADPCM Interrupt L (Read $20h : / Write : $21h)

ADPCM Interrupt H (Read $22h : / Write : $23h)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$20h	$21h	AIRQ7 0	AIRQ6 0	AIRQ5 0	AIRQ4 0	AIRQ3 0	AIRQ2 0	AIRQ1 0	AIRQ0 0	ADPCM Interrupt L -
$22h	$23h	- -	- -	- -	- -	- -	- -	- -	AIRQ8 0	ADPCM Interrupt H -

The ADPCM Interrupt L/H defines the FIFO address of the interrupt request flag.

ADPCM data is stored into the ADPCM FIFO register. When you start replaying with the AST bit, the data in the FIFO is being processed and erased. When remaining data lowers to or less than the amount set with the ADPCM interrupt during the ADPCM FIFO request is enabled, the ARQ bit is “1”. Then, the IRQ pin output turns to “L” and the ML2870 requests the external CPU to write the next data into the ADPCM FIFO.

Score Interrupt (Read $24h : / Write : $25h)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
$24h	$25h	-	SIRQ6	SIRQ5	SIRQ4	SIRQ3	SIRQ2	SIRQ1	SIRQ0	Score Interrupt
		-	0	0	0	0	0	0	0	-

Score data is stored into the SCORE FIFO register. When you start replaying with the AST bit, the data in the FIFO is being processed and erased. When remaining data lowers to or less than the amount set with the SCORE Interrupt during SCORE FIFO request is enabled, the SRQ bit is “1”. Then, the IRQ pin output turns to “L” and the ML2870 requests the external CPU to write the next data into the SCORE FIFO.

Event Interrupt (Read $26h : / Write : $27h)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$26h	$27h	-	-	-	-	EIRQ3	EIRQ2	EIRQ1	EIRQ0	Event Interrupt
		-	-	-	-	0	0	0	0	-

Event data is stored into the EVENT FIFO register. When you start replaying with the AST bit, the data on the FIFO is being processed and erased. When remaining data lowers to or less than the amount set with the EVENT Interrupt during EVENT FIFO request is enabled, the SRQ bit is “1”. Then, the IRQ pin output turns to “L” and the ML2870 requests the external CPU to write the next data into the EVENT FIFO.

Interrupt Enable (Read $28h : / Write : $29h)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$28h	$29h	- -	- -	- -	SYNCE 0	ISS 0	EIE 0	SIE 0	AIE 0	Interrupt Enable -

The interrupt enable register enables or disenables request for all FIFOs.

When each interrupt enable bit is “1”, the request signal of each FIFO is enabled. If residual data in each FIFO is lower than the amount set in the interrupt register, the next data is requested to the external CPU. When each interrupt enable bit is “0”, the request bit of each FIFO is fixed to “0” (no request).

Each interrupt enable bit is assigned as follows.

The AIE bit enables or disenables interrupt request of the ADPCM FIFO.

The SIE bit enables or disenables interrupt request of the SCORE FIFO.

The EIE bit enables or disenables interrupt request of the EVENT FIFO.

ISS bit is for inverting the interrupt signal from IRQ pin and for inverting values in request register.

The SYNCE bit enables or disables interrupt request for synchronous from sound generator.

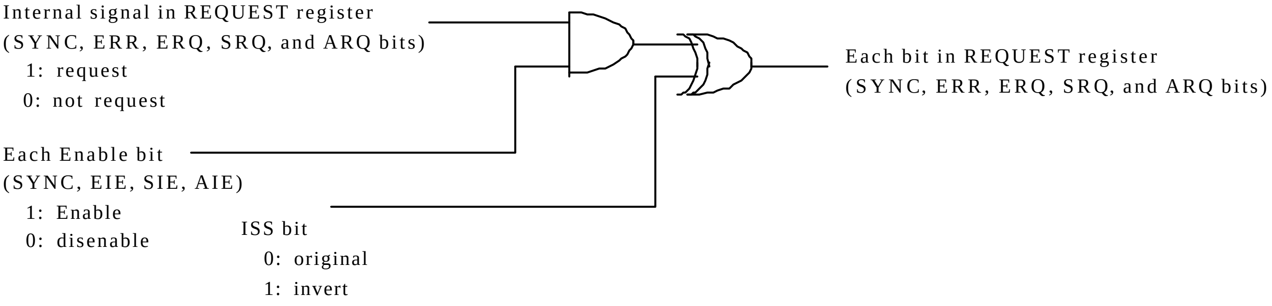

Internal signal in REQUEST register
(SYNC, ERR, ERQ, SRQ, and ARQ bits)
1: request
0: not request
Each Enable bit
(SYNC, EIE, SIE, AIE)
1: Enable
0: disenable
ISS bit
0: original
1: invert
Each bit in REQUEST register
(SYNC, ERR, ERQ, SRQ, and ARQ bits)

Table 13

I/F	Bus Interface / Serial Interface				Serial Interface Only	
ISS bit	SYNC / ERQ / SRQ / ARQ bit		IRQ pin		SYNC / ERQ / SRQ / ARQ bit	
	0	1	0	1	0	1
0	NO	REQUEST	NO	REQUEST	NO	REQUEST
1	REQUEST	NO	REQUEST	NO	REQUEST	NO

Request (Read $2Ah : / Write : $2Bh)

Interrupt Control Register										
INDEX		b07 (Initial)	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$2Ah	$2Bh	- -	- -	- -	SYNC 0	ERR 0	ERQ 0	SRQ 0	ARQ 0	REQUEST -

The Request register queries the external CPU.The ARQ bit, SRQ bit, and ERQ bits request subsequent data for musical scores or ADPCM data to the external CPU.

After these bits are set to “1”, set the interrupt enable register of each FIFO to “0”, and then write the subsequent data into the FIFO. After writing the data, return the Interrupt Enable Register to “1” to ready it for a next interrupt.

The request register is assigned to each request bit as follows.

The ARQ bit requests subsequent data for playing ADPCM audio.

The SRQ bit requests a subsequent musical score.

The ERQ bit requests subsequent event data.

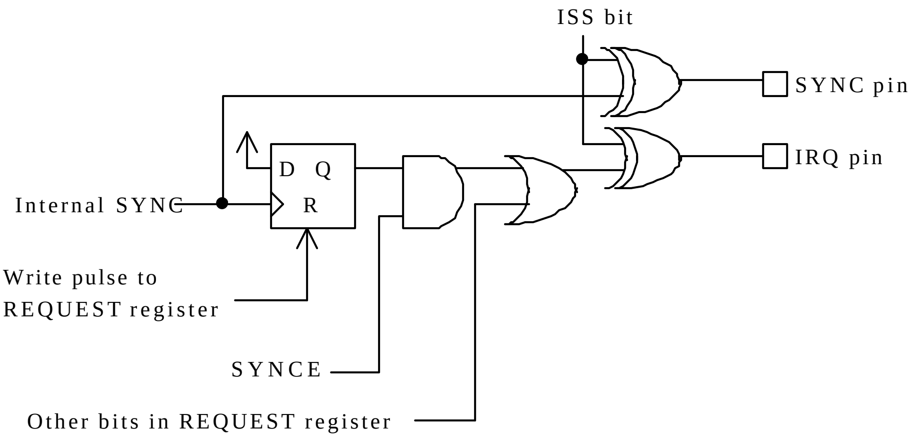
The ERR bit outputs “1” when an error occurs with the musical score. If ERR turns to “1”, stop playing the musical score. After setting the ST bit to “0”, the LSI will stop playing the music and reset the ERR bit to “0”.

Each request bit is for inverting the value according to ISS bit.

When set ISS bit to “0”, “1” means the request of next data

When set ISS bit to “1”, “0” means the request of next data.

SYNC bit is as same function as SYNC pin except for clearing the bit by write pulse of REQUEST register.



Status (Read $2Ch : / Write : inhibit)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$2Ch	-	- -	- -	- -	MMON 0	AMON 0	- -	- -	- -	STATUS -

The Status register has the status of the sequencer and the ADPCM synthesizer.

MMON is the sequencer flag. When MMON is “1”, the sequencer is active and the LSI plays music. When MMON is “0”, the sequencer is stopped and so is the music.

AMON is the flag of the ADPCM synthesizer. When AMON is “1”, the ADPCM synthesizer is active and the LSI plays ADPCM audio. When AMON is “0”, the ADPCM synthesizer is stopped and so is ADPCM audio.

MUSIC START (Read $30h : / Write : $31h)

Music & Voice Control Register									
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$30h	$31h	- -	- -	- -	- -	- -	- -	PAUSE 0	ST 0	MUSIC START

The MUSIC START register controls start and stop of playback. When the ST bit assumes "1", the LSI processes and erases data in the SCORE and EVENT FIFOs, and then the LSI plays notes though the sound generator. When ST assumes "0", the LSI stops playing music though the sound generator. If ST is forced to "0" during playback, clear the FIFOs with the SCLR and ECLR bits of the CLR register before playing the next music.

The PAUSE bit pauses playback of music. When PAUSE bit becomes "1" during the ST bit is "1", the LSI pauses playback. After set PAUSE bit to "1", write ALL SOUND OFF message to EVENT FIFO. Because it is possible not to erase all notes.

When reset PAUSE bit to "0", restart playback again.

ALL SOUND OFF message is 3 byte commands as following. As change value of "n" from "0" to "F", transfer total 48byte of commands to EVENT FIFO

0xBn,0x78,0x00

ADPCM START (Read $32h : / Write : $33h)

Music & Voice Control Register										
INDEX		b07	b06	b05	b04	b03	B02	b01	b00	NOTE
R	W									
$32h	$33h	- -	- -	- -	- -	- -	- -	MsyE 0	AST 0	ADPCM START

The ADPCM START register starts and stops playback. When ST assumes “1”, the LSI processes and erases data in the ADPCM FIFO (playback). When ST assumes “0”, the LSI stops the playback.

Please set the AST bit = “1”, AFTER the FIFO is put in ADPCM data. If playback is started when the FIFO is empty, noise can be played.

If AST is forced to “0” during playback, clear the FIFO with the ACLR bit of the CLR register before another playback.

MsyE bit is the register to select whether to play ADPCM sounds is synchronized with score data or not. When MsyE bit is “H”, ADPCM playback waits until a start trigger from the score FIFO. When MsyE bit is “L”, ADPCM playback commences.

Please write ADPCM data to the FIFO, before the start trigger from the score FIFO.

Fsamp (Read $34h : / Write : $35h)

Music & Voice Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$34h	$35h	- -	- -	- -	- -	F3 0	F2 0	F1 0	F0 0	Fsamp

The Fsamp register sets the sampling frequency and synthesis method of ADPCM audio.

It must be set before a playback.

Table 14: Synthesis methods and sampling frequencies of the Fsamp register

Value (F3-0)	Fsamp	Value (F3-0)	Fsamp
0	4.0kHz(4bit ADPCM2)	8	4.0kHz(2bit ADPCM2)
1	5.3kHz(4bit ADPCM2)	9	5.3kHz(2bit ADPCM2)
2	6.4kHz(4bit ADPCM2)	10	6.4kHz(2bit ADPCM2)
3	8.0kHz(4bit ADPCM2)	11	8.0kHz(2bit ADPCM2)
4	10.6kHz(4bit ADPCM2)	12	10.6kHz(2bit ADPCM2)
5	12.8kHz(4bit ADPCM2)	13	12.8kHz(2bit ADPCM2)
6	16.0kHz(4bit ADPCM2)	14	16.0kHz(2bit ADPCM2)
7	32.0kHz(4bit ADPCM2)	15	32.0kHz(2bit ADPCM2)

ADPCM PAN (Read $36h : / Write : $37h)

Music & Voice Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$36h	$37h	PL3 0	PL2 0	PL1 0	PL0 0	PR3 0	PR2 0	PR1 0	PR0 0	ADPCM PAN

The ADPCM PAN register sets the ADPCM volume of the left and right audio channels individually.

Table 15

PR3-0 PL3-0	Volume	PR3-0 PL3-0	Volume
0x00	0dB	0x08	-16dB
0x01	-2dB	0x09	-18dB
0x02	-4dB	0x0A	-20dB
0x03	-6dB	0x0B	-22dB
0x04	-8dB	0x0C	-24dB
0x05	-10dB	0x0D	-26dB
0x06	-12dB	0x0E	-28dB
0x07	-14dB	0x0F	MUTE

Volume (ADPCM) (Read $38h : / Write : $39h)

Music & Voice Control Register										
INDEX		b07	b06	B05	b04	b03	b02	b01	b00	NOTE
R	W									
$38h	$39h	-	-	-	ADVL4	ADVL3	ADVL2	ADVL1	ADVL0	Volume(ADPCM)
		-	-	-	0	0	0	0	0	

Volume of ADPCM reproduction is set up in 26 intervals. It is set to mute by 1Fh, and is set to the maximum volume by 0h

Table 16

Value (ADVL4-0)	Volume	Value (ADVL4-0)	Volume
0	0dB	13	-26dB
1	-2dB	14	-28dB
2	-4dB	15	-30dB
3	-6dB	16	-32dB
4	-8dB	17	-34dB
5	-10dB	18	-36dB
6	-12dB	19	-38dB
7	-14dB	20	-40dB
8	-16dB	21	-42dB
9	-18dB	22	-44dB
10	-20dB	23	-48dB
11	-22dB	24	-48dB
12	-24dB	25	Mute

Port mode (Read $40h : / Write : $41h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$40h	$41h	P7M 0	P6M 0	P5M 0	P4M 0	P3M 0	P2M 0	P1M 0	P0M 0	PORT MODE -

The port mode register selects the external CPU or ML2870 port assignment. When a bit in the port mode register is “0”, the external CPU controls the port assigned to that bit. When a bit in the port mode register is “1”, the ML2870 controls the port assigned to that bit. A musical score decides whether the port output is “1” or “0”.

NOTICE

On the QFN package only ports 4-0 are available. While the WCSP hosts all ports 7-0.

Table 17

bit	Assigned pins	Bit	Assigned pins
0 bit	PORT 0	4 bit	PORT 4
1 bit	PORT 1	5 bit	PORT 5
2 bit	PORT 2	6 bit	PORT 6
3 bit	PORT 3	7 bit	PORT 7

Port IO (Read $42h : / Write : $43h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$42h	$43h	PIO7 0	PIO6 0	PIO5 0	PIO4 0	PIO3 0	PIO2 0	PIO1 0	PIO0 0	PORT IO -

The PIO7-0 register decides whether a port is an output or an input port.

When a bit in the PIO7-0 register is “0”, the assigned port is an input port.

When a bit in the PIO7-0 register is “1”, the assigned port is an output port.

When a bit in the port mode register is “1”, the assigned port is a fixed output port.

Port (Read $44h : / Write : $45h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$44h	$45h	P7 1	P6 1	P5 1	P4 1	P3 1	P2 1	P1 1	P0 1	PORT -

The Port register describes 8 bit Bus data.

When the port IO register is “0”, an external device can write the value to the Port register.

When the port IO register is “1”, an external device can read the value from the Port register.

NOTICE

On the QFN package only ports 4-0 are available. While the WCSP hosts all ports 7-0.

When the Port mode register is “1”, the external CPU cannot read the value of Port register.

PWM mode (Read $46h : / Write : $47h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$46h	$47h	-	-	WVM	WPM	WDM	WCM	WBM	WAM	PWM MODE
		-	-	0	0	0	0	0	0	-

The PWM mode register selects the use of the PWM either for the external CPU or the ML2870 itself. When the PWM mode bit is "0", the CPU uses the PWM assigned bits.

When the PWM mode bit is "1", the ML2870 uses the PWM pin assigned bits.

Table 18

bit	Assigned pins
0 bit	PWMA pin
1 bit	PWMB pin
2 bit	PWMC pin
3 bit	PWMD pin
4 bit	PWM for panel
5 bit	PWM for vibrator

When PWM mode register is "1", density of PWM depends on velocity of following note in MIDI channel 10 (standard channel for drums and percussion)

Table 19: Percussion note number related to PWM pin

note number	Assigned PWM
96	PWMA
97	PWMB
98	PWMC
99	PWMD
100	PANEL
101	VIB

PWMA (Read $48h : / Write : $49h)

PWMB (Read $4Ah : / Write : $4Bh)

PWMC (Read $4Ch : / Write : $4Dh)

PWMD (Read $4Eh : / Write : $4Fh)

Panel (Read $50h : / Write : $51h)

VIB (Read $52h : / Write : $053h)

Table 20

PORT Control Register

INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$48h	$49h	WAE 0	WA6 0	WA5 0	WA4 0	WA3 0	WA2 0	WA1 0	WA0 0	PWMA
$4Ah	$4Bh	WBE 0	WB6 0	WB5 0	WB4 0	WB3 0	WB2 0	WB1 0	WB0 0	PWMB
$4Ch	$4Dh	WCE 0	WC6 0	WC5 0	WC4 0	WC3 0	WC2 0	WC1 0	WC0 0	PWMC
$4Eh	$4Fh	WDE 0	WD6 0	WD5 0	WD4 0	WD3 0	WD2 0	WD1 0	WD0 0	PWMD
$50h	$51h	WPE 0	WP6 0	WP5 0	WP4 0	WP3 0	WP2 0	WP1 0	WP0 0	Panel
$52h	$53h	WVE 0	WV6 0	WV5 0	WV4 0	WV3 0	WV2 0	WV1 0	WV0 0	Vib

The PWMA-D registers adjust the brightness of the LED driver in 128 steps. And directly drives 20mA current. The brightness of each PWM can be changed by the lower seven bits of each register. The MSB selects PWM enabled or disenabled. If set MSB to "1", PWM is active and if set MSB to "0", PWM is disabled.

The Panel register adjusts the brightness of an LCD front light in 128 steps and directly drives 100mA current.

The VIB register adjusts the intensity of the vibrator in 128 steps and directly drives 150mA current.

Pullup (Read $54h : / Write : $55h)

Port Control Register

INDEX		b07 (Initial)	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W									
$54h	$55h	$\overline{\text{PUP7}}$ 0	$\overline{\text{PUP6}}$ 0	$\overline{\text{PUP5}}$ 0	$\overline{\text{PUP4}}$ 0	$\overline{\text{PUP3}}$ 0	$\overline{\text{PUP2}}$ 0	$\overline{\text{PUP1}}$ 0	$\overline{\text{PLPU0}}$ 0	$\overline{\text{Pullup}}$ -

PUP7-0 register is to select pull-up resistor for each port. Whether used or not.

When PUP7-0 set to "1", the pull-up resistor is disconnection.

When $\overline{\text{PUP7-0}}$ set to "0", the pull-up resistor is connected.

PWM Output Select Register (Read $56h : / Write : $57h)

PORT Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$56h	$57h	$\overline{P7}$/PZ 0	$\overline{P6}$/PY 0	$\overline{P5}$/PV 0	$\overline{P4}$/PP 0	$\overline{P3}$/PD 0	$\overline{P2}$/PC 0	$\overline{P1}$/PB 0	$\overline{P0}$/PA 0	PWM Output Select

This register is to drive LED which need to be driven by more than 3.6V with a few components. When a value in the register is “0”, a port which is assigned to the bit is used for GPIO. When bit in the register is “1”, a port which is assigned to the bit is used for PWM output. The difference between what PWM outputs PORT and what PWM signal outputs PWM pin is shown the figure below. Each pin status can be selected individually. The following figures are shown how to drive a LED.

If it is necessary to connect LED to more than 3.6.V, PWM,VIB, and PANEL pins can’t be connected to high voltage directly. LED should be driven such the figure” Circuit for LED with more than 3.6v”.

On the other hand, if less than 3.6V for LED is enough, PWM pin can drive LED directly. The figure ”Circuit for LED with 3.6v or under” is referred to external circuit.

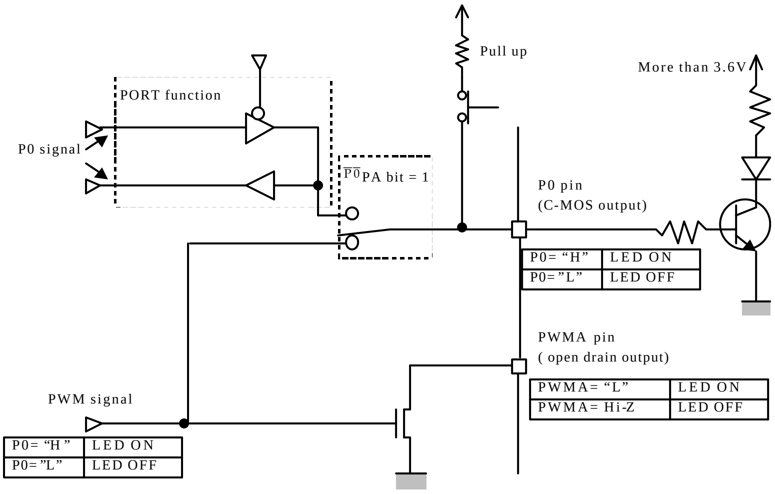
$\overline{P7}$/PZ bit and $\overline{P6}$/PY bit is for reserve. When the bits is “1”, P6 and P7 is fixed as “0” outputs.

(NOTE)

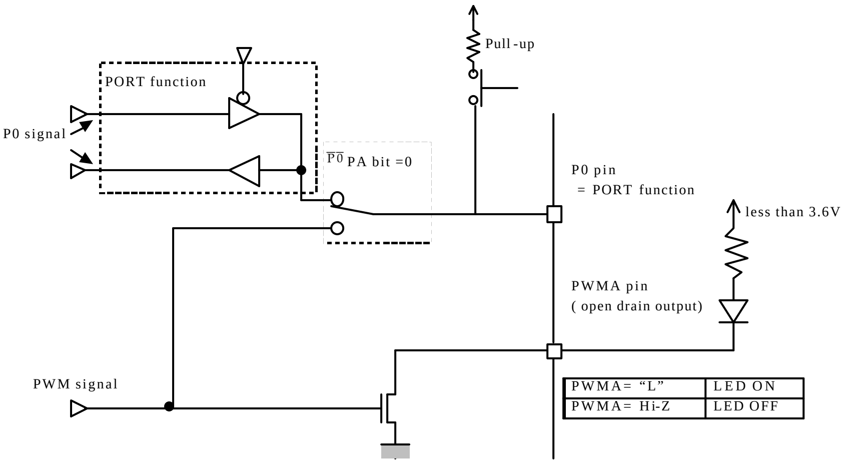
If PWM,VIB, or PANEL pin is connected to more than 3.6V directly, LSI would be broken possibly.

Pin name	**Port Output Select register**	**description**
P0	$\overline{P0}$/PA = 0	P0 outputs PORT 0 signal.
	$\overline{P0}$/PA = 1	P0 outputs PWMA signal.
P1	$\overline{P1}$/PB = 0	P1 outputs PORT 1 signal.
	$\overline{P1}$/PB = 1	P1 outputs PWMB signal.
P2	$\overline{P2}$/PC = 0	P2 outputs PORT 2 signal.
	$\overline{P2}$/PC = 1	P2 outputs PWMC signal.
P3	$\overline{P3}$/PD = 0	P3 outputs PORT 3 signal.
	$\overline{P3}$/PD = 1	P3 outputs PWMD signal.
P4	$\overline{P4}$/PP = 0	P4 outputs PORT 4 signal.
	$\overline{P4}$/PP = 1	P4 outputs Panel signal.
P5	$\overline{P5}$/PV = 0	P5 outputs PORT 5 signal.
	$\overline{P5}$/PV = 1	P5 outputs VIB signal.

<Fig: Circuit for LED with more than 3.6v >



<Fig: Circuit for LED with 3.6v or under >



Note: When PWM is controlled by PORT pin

(In case that used as “Fig: Circuit for LED with 3.6v or under”, on the previous page)

Pull-up register is enabled at the default. There is a current flow through the pull-up register (min 20kΩ). Please set the registers for PORT pin as follows, right after the reset.

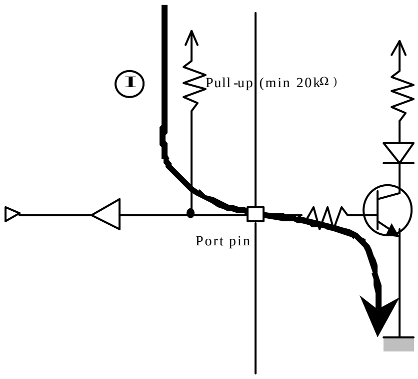
[Register setting]

Pull up register : off

PWM Output Select register : PWM

PORT IO register : Output

Figure: Equivalent circuit of default Port pins



Audio Volume (Read $62h : / Write : $63h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$62h	$63h	VR3 0	VR2 0	VR1 0	VR0 0	VL3 0	VL2 0	VL1 0	VL0 0	Audio Volume -

Audio Volume register is for changing audio volume to mix between sound generator and ADPCM. Please use the function for volume control of the terminal.

In the portion of more than –12 dB, it is possible for analog output to saturate. But there is no problem at ringtone. Therefore, usage of more than –12dB is recommended due to the improvement of S/N.

Table 21

PR3-0 PL3-0	Volume	PR3-0 PL3-0	Volume
0x00	0dB	0x08	-24dB
0x01	-2.5dB	0x09	-26.5dB
0x02	-6dB	0x0A	-30dB
0x03	-8.5dB	0x0B	-32.5dB
0x04	-12dB	0x0C	-36dB
0x05	-14.5dB	0x0D	-38.5dB
0x06	-18dB	0x0E	-42dB
0x07	-20.5dB	0x0F	MUTE

VR3-0 bit: Change the volume for AOUTR pin.

VL3-0 bit: Change the volume for AOUTL pin.

Analog Power Down (Read $66h : / Write : $67h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$66h	$67h	BIASR 0	PDR 1	ENL2R 0	ENR2R 1	BIASL 0	PDL 1	ENR2L 0	ENL2L 1	Analog Power Down -

Analog Power Down register specifies enabling or disenabling power down of analog part.

The detail is shown below.

BIASR: Select enabling or disenabling voltage bias to reduce pop noise when reset and set power down of AOUTR pin.

PDR: Select enabling or disenabling audio output from AOUTR pin.

ENR2R: Enable output of right audio output from AOUTR pin.

ENL2R: Enable output of left audio output from AOUTR pin.

Set up of ENL2R/ENR2R When the ENL2R=0 are selected, it is enable to output Right channel audio data from AOUTR pin, regardless of ENR2R's register.

BIASL: Select enabling or disenabling voltage bias to reduce pop noise when reset and set power down of AOUTL pin.

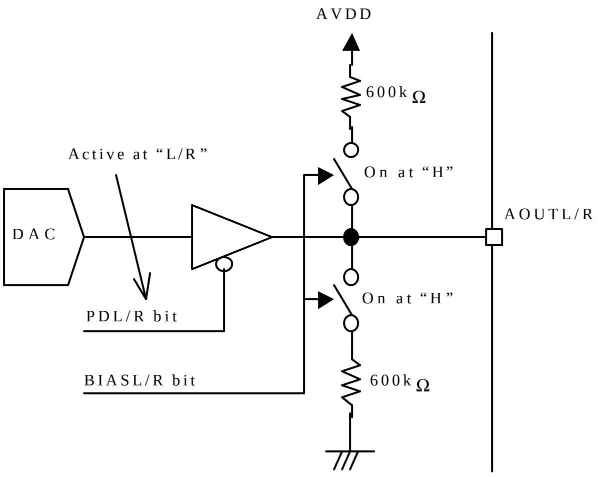
PDL: Select enabling or disenabling audio output from AOUTL pin.

ENL2L: Enable output of left audio output from AOUTL pin.

ENR2L: Enable output of right audio output from AOUTL pin.

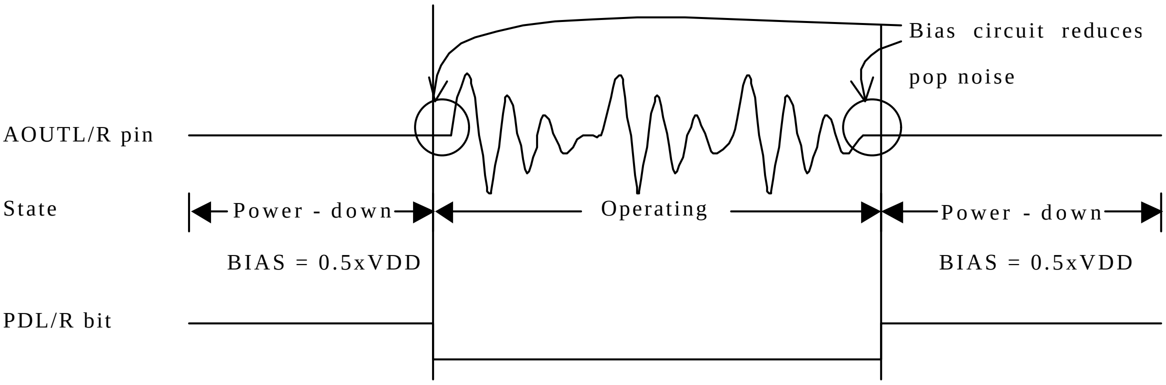
Set up of ENR2L/ENL2L When the ENR2L=0 are selected, it is enable to output Left channel audio data from AOUTL pin, regardless of ENL2L's register.

The LSI includes following circuit for reducing pop noise.



Please refer to the figures below for the difference analog level of BIASL/R bit.

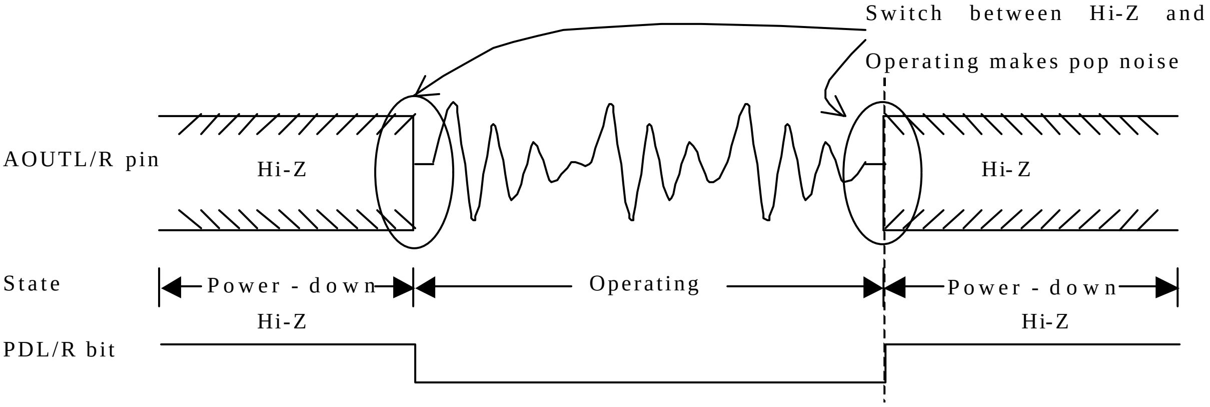
<BIASL/R bit = 1>



The voltage of AOUTL/R pin in Hi-Z is set approximate value in Operating. It reduces pop noise at switching Hi-Z – Operating.

NOTE : BIAS circuit can NOT delete pop noise completely. Please make sure that it's in tolerance level.

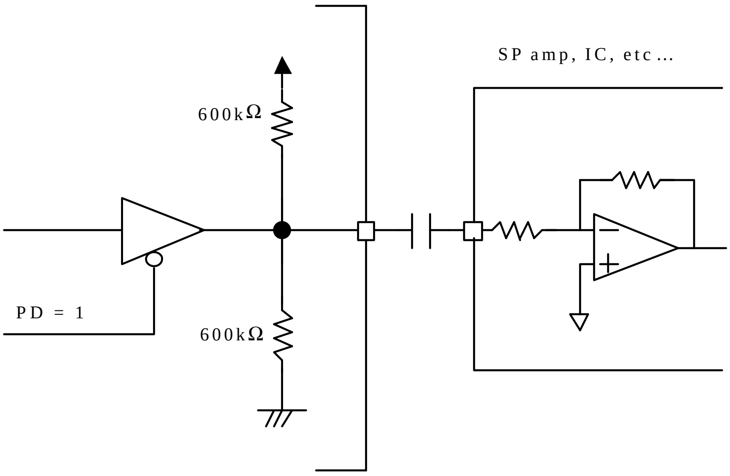
<BIASL/R bit = 0>



For the voltage of AOUTL/R pin is indeterminate in Hi-Z, switch between Hi-Z and Operating makes major pop noise.

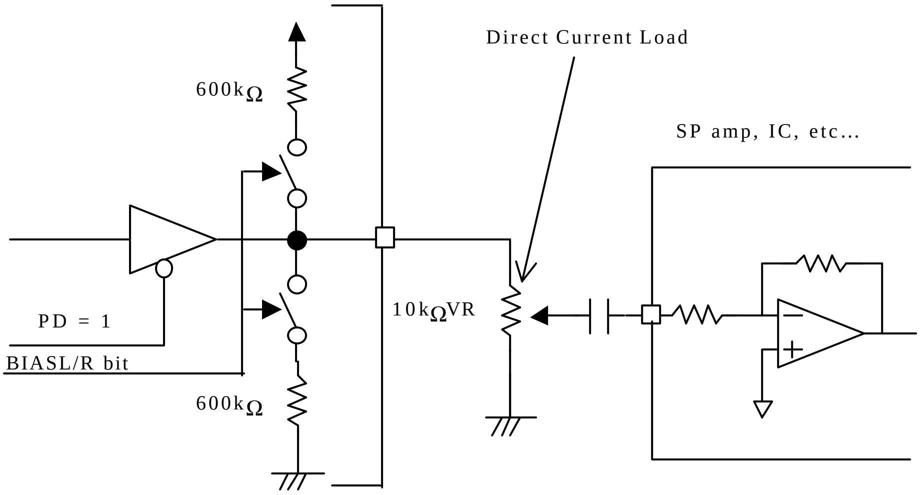
Speaker amplifier should be connected to the LSI as follows.

Recommended circuit = connecting SP amplifier with AC coupling.



BIAS Level is set about 0.5 x Vpp

NOTE: In the case of following circuit, the BIAS circuit for reducing pop noise doesn't work properly. Therefore set the BIASL/R bit = 0, and reduce pop noise by adding outside circuit.



AOUT Invert (Read $68h : / Write : $69h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$68h	$69h							AORINV 0	AOLINV 0	AOUT Invert (for BTL mode)

AOUT Invert register specifies the phase of analog output from AOUTL/R pins. When the register is set to BTL output, PSRR can be improved as more than 6dB. BTL Output mode can be configured by the setting below.

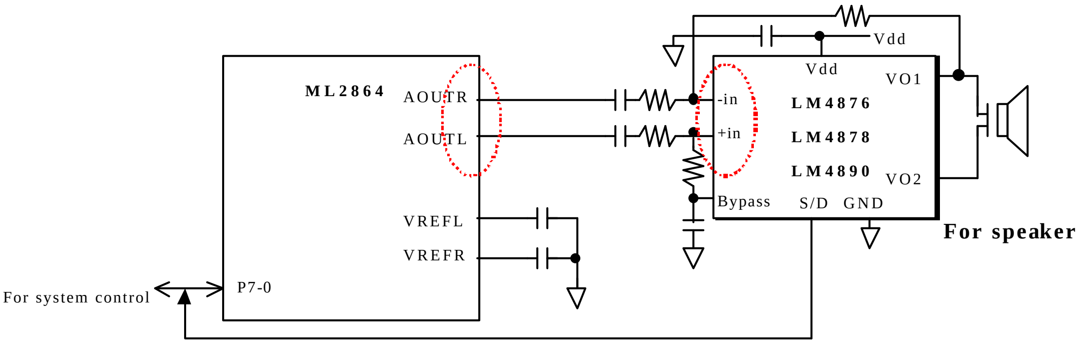
- AORINV bit = 1, AOLINV bit = 0
- all bit of ENL2R,ENR2R,ENR2L,ENL2L in “Analog Power Down” register is set to “H”.
- Set same value to left channel and right channel in “Audio Volume” register

AOLINV: Select the phase with AOUTL-pin. When the AOLINV=1 are selected, analog signal is inverted which outputted form AOUTL-pin.

AORINV: Select the phase with AOUTR-pin. When the AORINV=1 are selected, analog signal is inverted which outputted form AOUTR-pin.

Set up of AOLINV/AORINVEVENT DATA FORMAT

The EVENT FIFO and the event mode of the score FIFO can enter the commands of the "MIDI IMPLEMENTATION CHART" below and the "Exclusive Format".



Please follow the formats when entering the data into the ML2870.

MIDI IMPLEMENTATION CHART

Table 22

Function name		Recognized	Remark
Basic Channel	POWER ON	1-16	
Mode	Message	Mode 3 Omni OFF, Poly	
	Altered	This is not included into the function.	
Note Number		0-127	
	True Voice	0-127	
Velocity	Note ON	This is included into the function. 9nH v = 1-127	
	Note Off	9nH v = 0, 8nH v = *1	
After Touch	Key's	X	
	Ch's	O	
Pitch Bender		O	Bend range: Depend on pitch bend sensitivity max 1 octave default 2 semi-tone
Control Change	1	O	Modulation
	6,38	O	Data entry
	7	O	Volume
	10	O	Pan
	11	O	Expression
	64	O	Hold 1 (Sustain)
	98,99	O	NRPN LSB, MSB
	100,101	O	NRPN LSB, MSB
	121	O (next : 0)	Reset all control
	120	O (next: 0)	All sounds off
	123	O (next: 0)	All notes off
Program Change		0-127	
System Exclusive			
System Common	Song Position	X	
	Song Select	X	
	Tune	X	
System Real Time	Clock	X	
	Commands	X	
Aux Message	Local ON/OFF	X	
	All Note Off	X	
	Active Sense	X	
	Reset	X	

Mode 1:Omni On, Poly	Mode 2:Omni On, Mono
Mode 4:Omni Off, Poly	Mode 4:Omni Off, Mono

EXCLUSIVE FORMAT

Table 23

Command	1	2	3	4	5	6	7	8	9	10	Remark
Transpose	0xf0	0x06	0x5d	0x0e	0x08	0x10	0xkk	0xf7	-	-	kk = transpose value : -6 ~ +5
Main volume	0xf0	0x06	0x5d	0x0e	0x08	0x11	0xvv	0xf7	-	-	vv = main volume : 0 ~ 127
Touch correct	0xf0	0x06	0x5d	0x0e	0x08	0x13	0xtt	0xf7	-	-	tt = touch correct : 0 ~ 127
Set tempo message	0xf0	0x07	0x5d	0x0e	0x08	0x14	0xtt1	0xtt2	0xf7	-	tt1 and tt2 = tempo value
Parameters change	0xf0	0x06	0x5d	0x0e	0x08	0x15	0xsw	0xf7	-	-	Sw : synchronous mode
Effective sounds	0xf0	0x08	0x5d	0x0e	0x08	0x18	0xch	0xtl	0xth	0xf7	ch = channel / tl,th = tone number
Relative tempo	0xf0	0x06	0x5d	0x0e	0x08	0x19	0xrr	0xf7	-	-	0xrr = relative tempo x ± 5%
GM System on	0xf0	0x05	0x7e	0x7f	0x09	0x01	0xf7	-	-	-	Reset Sound generator
Master Expression	0xf0	0x06	0x5d	0x0e	0x08	0x1b	ee	0xf7	-	-	me = 0 ~ 127
Master Pan	0xf0	0x06	0x5d	0x0e	0x08	0x1c	pp	0xf7	-	-	mp = 0(left) ~ 64(center) ~ 127(right)
Pile Voice	0xf0	0x07	0x5d	0x0e	0x08	0x7c	dco	0x00	0xf7	-	dco = 0 ~ 32

Transpose (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x10, 0xkk, 0xf7)

Table 24

Command	1	2	3	4	5	6	7	8	9	10
Transpose	0xf0	0x06	0x5d	0x0e	0x08	0x10	0xkk	0xf7	-	-

Transpose, an 8-byte command, transposes musical notes. The transpose function is available for the note after the LSI recognizes this command. If the LSI receives this command during processing of notes, it is ineffective.

If the transposition result is less than 0 or more than 127, the LSI changes to the note numbers that can be played an octave higher or lower.

Table 25

0xkk	Transpose	0xkk	Transpose
0x46	-6	0x00	0
0x45	-5	0x01	1
0x44	-4	0x02	2
0x43	-3	0x03	3
0x42	-2	0x04	4
0x41	-1	0x05	5

Main volume (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x11, 0xvv, 0xf7)

Table 26

Command	1	2	3	4	5	6	7	8
Main volume	0xf0	0x06	0x5d	0x0e	0x08	0x11	0xvv	0xf7

Main volume is 8 bytes command change main volume of sound generator.

Touch correct (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x13, 0xtt, 0xf7)

Table 27

Command	1	2	3	4	5	6	7	8
Touch correct	0xf0	0x06	0x5d	0x0e	0x08	0x13	0xtt	0xf7

Touch correct is an 8-byte command to adjust the velocity of music data. When playing back as ringing tone and the volume is low, it sets the data to be added to the velocity.

Set tempo message (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x14, 0xtt1, 0xtt2, 0xf7)

Table 28

Command	1	2	3	4	5	6	7	8	9
Set tempo message	0xf0	0x06	0x5d	0x0e	0x08	0x14	0xtt1	0xtt2	0xf7

Set tempo message is a 9 bytes command to change tempo of song by force. value of tempo is from 30 to 500 in score tempo. (ex.) 120 is 500ms at a quarter note.

tt2 and tt1 is calculated like follows.

tt2 = tempo >> 7, tt1 = tempo & 0x7F.

Parameters change (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x15, 0xsw, 0xf7)

Table 29

Command	1	2	3	4	5	6	7	8
Parameters change	0xf0	0x06	0x5d	0x0e	0x08	0x15	0xsw	0xf7

Parameter change, an 8-byte command, which decides over the priority concerning the exclusive parameter of the FIFO.

Parameter change command affects only program change and control change.

Table 30

Sw bit	Remarks
0	Parameter into SCORE FIFO is available.
1	Parameter into EVENT FIFO is available.

Sound effects (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x18, 0xch, 0xtn, 0xf7)

Table 31

Command	1	2	3	4	5	6	7	8	9	10	Remark
Effective sounds	0xf	0x08	0x5d	0x0e	0x08	0x18	0xch	0xtl	0xth	0xf7	ch = channel / tl,th = tone number

Effective sounds is a 10 bytes command to output effective sound. The ch byte is to indicate the MIDI channel to output the sound effect. The table of effective sound by tl and th is shown below.

Table 32

th<<7 +tl	Remark
0-127	GM sound set
136	Square wave 1 (long)
137	Square wave 1 (short)
138	Square wave 1 (continuous)
139	Sin wave 1 (long)
140	Sin wave 1 (short)
141	Sin wave 1 (continuous)

Relative tempo (0xf0, 0x06, 0x5d, 0x0e, 0x08, 0x19, 0xrr, 0xf7)

Table 33

Command	1	2	3	4	5	6	7	8
Relative tempo	0xf0	0x06	0x5d	0x0e	0x08	0x19	0xrr	0xf7

Relative tempo is an 8 bytes command to change tempo relatively to compare with original tempo.

The range of tempo is 20 to 500.

If tempo is more than 500, tempo is fixed to 500. If tempo is less than 20, tempo is fixed to 20.

GM System on (0xf0 0x05 0x7e 0x7f 0x09 0x01 0xf7)

Table 34

Command	1	2	3	4	5	6	7	8
GM System on	0xf0	0x05	0x7e	0x7f	0x09	0x01	0xf7	-

“GM system on” resets the parameter of sound generator, ex. Control change , program number , pitch bend and so on.

Master Expression (0xf0 0x06 0x5d 0x0e 0x08 0x1b ee 0xf7)

Table 35

Command	1	2	3	4	5	6	7	8
Master Expression	0xf0	0x06	0x5d	0x0e	0x08	0x1b	ee	0xf7

Master expression sets substitute volume, by 0~127. It works as Main Volume. Master Expression is usually used to add intonation on certain timber.

Master Pan (0xf0 0x06 0x5d 0x0e 0x08 0x1c pp 0xf7)

Table 36

Command	1	2	3	4	5	6	7	8
Master Pan	0xf0	0x06	0x5d	0x0e	0x08	0x1c	pp	0xf7

Master Pan sets panpot, by 0(left)~64(center)~127(right).

Pile Voice (0xf0 0x06 0x5d 0x0e 0x08 0x7c dco 0x00 0xf7)

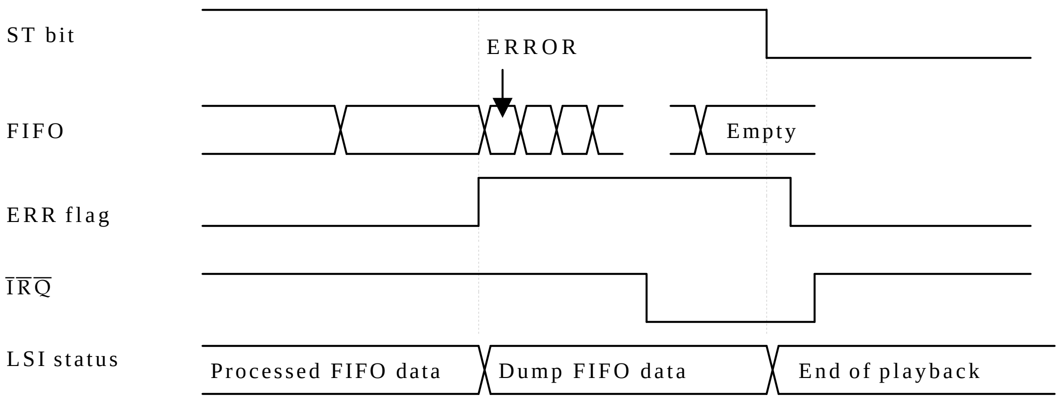
Table 37

Command	1	2	3	4	5	6	7	8	9
Pile Voice	0xf0	0x07	0x5d	0x0e	0x08	0x7c	dco	0x00	0xf7

Pile voice is to enlarge dynamic range of each voice, if contents don’t have enough polyphony for loudness. Pile voice entry is specified that polyphony for each voice is changed. For example, If contents have only 8 polyphony, “dco” can be set to 0x04. And each voice consume 4 polyphony and maximum number of polyphony is changed to only 8. But volume of Music is loud. Since it is impossible to increase volume at a few polyphony, this command is available to make volume loud

Processing Music Data Error

If music data contains any erroneous data, the LSI cannot recognize data other than the error data. In such an event, the LSI enters its error processing mode and outputs "H" on the ERR bit.
Set the ST bit to "0" to stop playing once the ERR bit is turned "H".



TONE LIST

The note range of each tone is from C0 to C8. The range of note number is from 12 to 108.

When input the note number beyond the range, ML2870 changes to the nearest note number to be played by octave unit.

Table 38

GM	Poly	GM Tone Map	GM	Poly	GM Tone Map
0	1	Acoustic Grand Piano	32	1	Acoustic Bass
1	1	Bright Acoustic Piano	33	1	Electric Bass (finger)
2	2	Electric Grand Piano	34	1	Electric Bass (pick)
3	2	Honkey-tonk Piano	35	1	Fretless Bass
4	1	Electric Piano 1	36	1	Slap Bass 1
5	1	Electric Piano 2	37	1	Slap Bass 2
6	1	Harpsichord	38	1	Synth Bass 1
7	1	Clavi	39	1	Synth Bass 2
8	1	Celesta	40	1	Violin
9	1	Glockenspiel	41	1	Viola
10	2	Music Box	42	1	Cello
11	1	Vibraphone	43	1	Contrabass
12	1	Marinmba	44	1	Tremolo Strings
13	1	Xylophone	45	1	Pizzicato Strings
14	1	Tubular Bells	46	1	Orchestral Harp
15	2	Dulcimer	47	1	Timpani
16	2	Drawbar Organ	48	1	String Emsemble 1
17	2	Percussive Organ	49	1	String Emsemble 2
18	2	Rock Organ	50	1	Synth String 1
19	2	Church Organ	51	2	Synth String 2
20	1	Reed Organ	52	1	Choir Aahs
21	2	Accordion	53	1	Voice Oohs
22	1	Harmonica	54	2	Synth Vox
23	2	Tango Accordion	55	2	Orchestra Hit
24	1	Acoustic Guitar (nylon)	56	1	Trumpet
25	1	Acoustic Guitar (steel)	57	1	Trombone
26	1	Electric Guitar (jazz)	58	1	Tuba
27	1	Electric Guitar (clean)	59	1	Muted Trumpet
28	1	Electric Guitar (muted)	60	2	French Horn
29	1	Overdriven Guitar	61	1	Brass Section
30	1	Distortion Guitar	62	2	Synth Brass 1
31	1	Guitar harmonics	63	2	Synth Brass 2

Table 39

GM	Poly	GM Tone Map	GM	Poly	GM Tone Map
64	1	Soprano Sax	96	2	Fx1 (rain)
65	1	Alto Sax	97	2	Fx2 (soundtrack)
66	1	Tenor Sax	98	2	Fx3 (crystal)
67	1	Baritone Sax	99	2	Fx4 (atmosphere)
68	1	Oboe	100	2	Fx5 (brightness)
69	1	English Horn	101	2	Fx6 (goblins)
70	1	Bossoon	102	2	Fx7 (echoes)
71	1	Clarinet	103	2	Fx8 (sci-fi)
72	1	Piccolo	104	1	Sitar
73	1	Flute	105	1	Banjo
74	1	Recorder	106	1	Shamisen
75	1	Pan Flute	107	1	Koto
76	2	Blown Bottle	108	1	Kalimba
77	2	Shakuhachi	109	2	Bag pipe
78	1	Whistle	110	2	Fiddle
79	1	Ocarina	111	1	Shanai
80	2	Lead 1 (square)	112	1	Tinkle Bell
81	2	Lead 2 (sawtooth	113	1	Agogo
82	2	Lead 3 (calliope)	114	2	Steel Drums
83	2	Lead 4 (chiff)	115	1	Woodblock
84	2	Lead 5 (charang)	116	1	Taiko
85	2	Lead 6 (voice)	117	1	Melodic Tom
86	2	Lead 7 (fifths)	118	2	Synth Drum
87	2	Lead 8 (bass + lead)	119	1	Reverse Cymbal
88	2	Pad 1 (new age)	120	1	Guitar Fret Noise
89	2	Pad 2 (warm)	121	1	Breath Noise
90	2	Pad 3 (polysynth)	122	2	Seashore
91	2	Pad 4 (choir)	123	1	Bird Tweet
92	2	Pad 5 (bowed)	124	1	Telephone Ring
93	2	Pad 6 (metallic)	125	1	Helicopter
94	2	Pad 7 (halo)	126	2	Applause
95	2	Pad 8 (sweep)	127	1	Gunshot

Percussion MapNote 96-101 is assigned as PWM1-4, PANEL, and VIB pins. The value of velocity is specified as the brightness

Table 40

No.	Percussion name	No	Percussion Name	No	Percussion Name
35	Acoustic Bass Drum	59	Ride Cymbal2	96	PWM1
36	Bass Drum1	60	Hi Bongo	97	PWM2
37	Side Stick	61	Low Bongo	98	PWM3
38	Acoustic Snare	62	Mute Hi Conga	99	PWM4
39	Hand Clap	63	Open Hi Conga	100	PANEL
40	Electric Snare	64	Low Conga	101	VIB
41	Low Floor Tom	65	High Timbale		
42	Closed Hi-Hat	66	Low Timbale		
43	High Floor Tom	67	High Agogo		
44	Pedal Hi-Hat	68	Low Agogo		
45	Low Tom	69	Cabasa		
46	Open Hi-Hat	70	Maracas		
47	Low-Mid Tom	71	Short Whistle		
48	Hi-Mid Tom	72	Long Whistle		
49	Crash Cymbal1	73	Short Guiro		
50	High Tom	74	Long Guiro		
51	Ride Cymbal1	75	Clavas		
52	Chinese Cymbal	76	Hi Wood Block		
53	Ride Bell	77	Low Wood Block		
54	Tambourine	78	Mute Cuica		
55	Splash Cymbal	79	Open Cuica		
56	Cowbell	80	Mute Triangle		
57	Crash Cymba 2	81	Open Triangle		
58	Vibraslap				

REVISION HISTORY

Table 41

Date	Page	Notes	Revision
Apr.12.2003	-	1st version	00.00.01
Mar.6.2003	37-94	Header title is corrected to “ML2864”. wrong : ML2870	00.00.02

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.
5. Neither indemnity against nor license of a third party’s industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party’s right which may result from the use thereof.
6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.

   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.
7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.
8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Copyright 2003 Oki Electric Industry Co., Ltd.